

A Tunable CMOS Continuous-Time Filter Designed for a 5.8 GHz ETC Demodulator

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Abstract. 5.8 GHz is specified as the operating frequency of the electronic tolling collection (ETC) system in the new national highway network in China. A low power, robust radio frequency receiver is the key design challenge in such a system. A 3rd order butterworth low-pass filter with tunable pass-band designed for the ETC receiver was presented in this work. The design is based on a single operational amplifier in order to reduce the overall power consumption. The filter was implemented in standard CMOS 0.18 μm technology. Simulation shows that the design achieves a maximum 3-dB bandwidth of 2 MHz with 0 dB insertion loss, while the power consumption is only $\sim 200 \mu\text{W}$.

Keywords: ETC receiver, Continuous-time filter, tunable pass-band, operational amplifier.

1 Introduction

Traffic congestion is becoming a problem in most major cities in China. One way to alleviate the traffic pressure is to construct urban intelligent traffic control system by employing information and wireless communication technologies. Among those, electronic tolling collection (ETC) system, which allows vehicles to pass through a toll booth without stopping, is one of the most effective methods. According to the Chinese standard of Dedicated Short Range Communications (DSRC) [1], the operating frequencies of the ETC system is set to be 5.8- 5.9 GHz.

A 5.8 GHz Radio Frequency (RF) low power receiver is essential for an ETC system, and the directional conversion architecture is generally adopted due to its simplicity and robustness. Currently, Shenzhen University is developing such a receiver. As shown in Fig.1, received signal is first down-converted to an intermediate frequency of 10 MHz. By using this method, the high DC offset generally presented at the receiver baseband, which is primarily caused by the leakage from the local oscillator to the receiver front-end, is avoided. A band-pass filter (BPF) and a log-amplifier / received signal strength

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indicator (Log-Amp/RSSI) are used to extract and amplify the IF signal, followed by a low-pass filter, an envelope detector, and a comparator with hysteresis for data recover. The receiver is required to recover data sequence up to 2 Mbit/s.

This work focuses on the low-pass filter in the ETC receiver. Because the maximum data rate (~2 Mb/s) is far below the 10 MHz IF frequency, a filter with 3rd order response is sufficient to isolate the recovered data from the down-converted signal. Butterworth type is chosen because it can provide the most flat in-band response, with a good compromise between gain, phase and signal delay [2]. The implemented filter is based on a single operational amplifier (OPAMP) in order to reduce the total circuit power consumption.

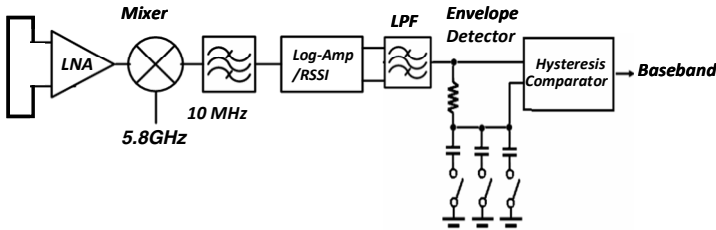


Fig. 1. Architecture of 5.8 GHz RF ETC receiver under developing in Shenzhen University

The paper is organized as follows: The CMOS operational amplifier design is presented in section 2, with discussion of design issues including the amplifier gain and bandwidth. The low pass filter was then implemented using the operational amplifier and several passive components, and the filter design procedure is presented in section 3. The filter is designed using standard CMOS 0.18 μm technology, and is validated under the Zeni IC design environment. The simulation results are presented in section 4, and the concluding remarks are given in Section 5.

2 Two-Stage OPAMP Design

Since the output signal from the Log-Amp/RSSI block is differential while a single-ended input is required for the envelope detector, a two-stage OPAMP that achieves both differential to single-ended conversion and signal amplification is implemented in this design. The first stage functions as a differential-to-single-ended converter, and only provides moderate gain. A common-source structure is added as the second stage for enhanced gain, and at the same time buffers the amplified signal. In addition, a R-C compensation network is added between the two stages in order to achieve a large unity-gain-bandwidth. The detailed schematic of the OPAMP is given in Fig.2.

The first stage of the OPAMP consists of 5 transistors. M_5 provides the necessary DC bias current I_{SS} . M_3 and M_4 form the input pair, and M_1 , M_2 make up of the active current loads. The input common mode voltage is defined as V_{in} . When V_{in} increases progressively and is larger than the threshold voltage of the M_3 , M_4 , they start to turn on and enter the active region. The minimum value of V_{in} that ensures all the transistors of the first stage operating in the active region is:

$$V_{in} = \sqrt{\frac{I_{ss}}{\mu_n C_{ox} (\frac{W}{L})_1}} + V_{TH3} + \sqrt{\frac{2I_{ss}}{\mu_n C_{ox} (\frac{W}{L})_5}}, \tag{1}$$

where V_{TH3} is the threshold voltage of M_3 and M_4 , $(W/L)_1$ and $(W/L)_5$ represent the device sizes of M_1 and M_5 , respectively.

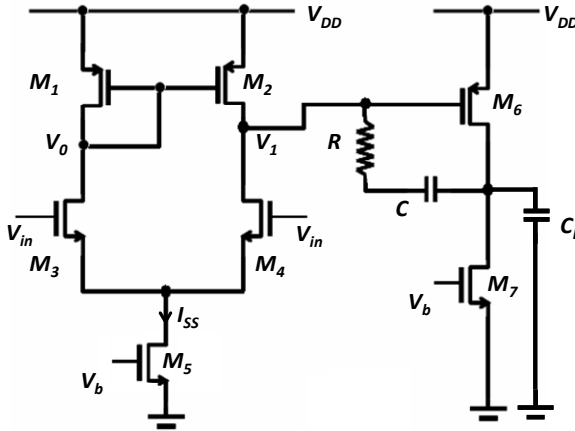


Fig. 2. Detailed schematic of the OPAMP

The outputs of the first stage, which are defined as V_0 and V_1 , decrease with the increasing of V_{in} , and M_3 and M_4 can enter the triode region if V_{in} is too high. In order to maintain all transistors operating in the active region, the maximum V_{in} should satisfy equation (2).

$$V_{in} = V_{DD} - \sqrt{\frac{I_{ss}}{\mu_p C_{ox} (\frac{W}{L})_1}} - |V_{TH1}| + V_{TH3}, \tag{2}$$

where V_{TH1} is the threshold voltage of M_1 and M_2 .

With V_{in} set to be between the limits defined as in (1) and (2), V_0 and V_1 are identical to the 1st order, and can be written as:

$$V_0 = V_1 = V_{DD} - |V_{GS1}| = V_{DD} - \sqrt{\frac{I_{ss}}{\mu_p C_{ox} (\frac{W}{L})_1}} - |V_{TH1}| \tag{3}$$

The common mode voltage gain of the first OPAMP stage under the proper bias condition can then be derived as in (4)

$$A_{CM} \approx \frac{-\frac{1}{2g_{m1,2}} \parallel \frac{r_{01,2}}{2}}{\frac{1}{2g_{m3,4}} + r_{05}} = -\frac{1}{1 + 2r_{05}g_{m3,4}} \frac{g_{m3,4}}{g_{m1,2}} \tag{4}$$

,where $r_{01,2}$ and r_{05} are the channel resistances of M_1/M_2 and M_5 , $g_{m1,2}$ is the transconductance of M_1/M_2 , and $g_{m3,4}$ is the transconductance of M_3 or M_4 .

The differential small signal gain of the first stage can be estimated using (5),

$$A_{DM} = g_{m3,4}(r_{02} \parallel r_{04}), \quad (5)$$

where r_{02} and r_{04} are the channel resistance of M_2 and M_4 , respectively.

Based on (4) and (5), the common mode rejection ratio (CMRR) can be written as

$$CMRR = \left| \frac{A_{DM}}{A_{CM}} \right| = (1 + 2r_{05}g_{m3,4})g_{m1,2}(r_{02} \parallel r_{04}) \quad (6)$$

From (6), it indicates that the input pairs M_3 and M_4 should use large (W/L) ratio for high differential small signal gain and CMRR value. However, since the first stage output voltage, V_I , is also the DC bias voltage of the second stage, the device size of M_3 and M_4 can not be determined independently, and the W/L of M_5 , thus the bias current I_{SS} , must be included in the design procedure in order for transistors in the second stage to operate properly in the active region.

An R-C compensation configuration is added between the two amplifying stages. This configuration moves the inter stage pole towards the origin and pushes away the output pole, which allows a much greater gain bandwidth product (GBW) than the structure that merely connects the compensation capacitor from one node to ground [3]. In addition, the resistor R in series with the capacitor C introduces a right half plane zero, $g_{m6}/(C+C_{GD6})$, which could be used to cancel the second system pole. The relation of R , C and C_L for pole-zero cancellation to occur is given in (7).

$$\frac{1}{C(g_{m6}^{-1} - R)} = \frac{-g_{m6}}{C_L}, \quad (7)$$

where g_{m6} is the transconductance of M_6 , and C_L is the load capacitor of the OPAMP.

With the R-C frequency compensation, the small signal gain of the completed operational amplifier can be written as

$$\frac{V_{out}}{V_{in}} = g_{m4}(r_{02} \parallel r_{04}) \frac{\frac{1}{R + \frac{1}{SC}} - g_{m6}}{\frac{1}{r_0} + \frac{1}{R + SC}} \quad (8)$$

3 OPAMP-Based 3rd Order Low-Pass Filter with Tunable Pass-Band

A butterworth architecture is used to implement the low pass filter because of its flat in-band response. In order to provide flexibility to the completed filter, tunability is introduced by integrating a programmable capacitor array. The proposed architecture of the low pass filter is given in Fig.3.

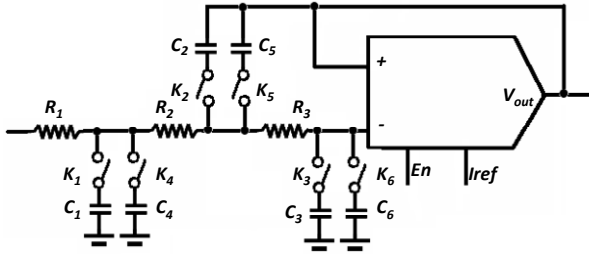


Fig. 3. Architecture of the OPAMP-based 3rd order low-pass filter

The design is based on the OPAMP discussed in the previous section, and totally 9 passive components, including a programmable capacitor array (C_1 and C_4 , C_2 and C_5 , C_3 and C_6) and three resistors (R_1 , R_2 , and R_3), are utilized. Using this scheme, the 3 dB cut-off frequency of the filter can be tuned by switches $K_1 - K_6$. When all switches are closed, the filter cut-off frequency is set to 1 MHz, and the cut-off frequency is set to 2 MHz if only K_1 , K_2 and K_3 are open.

The frequency domain transfer function of the filter can be derived as (9).

$$\begin{aligned}
 H(\omega) &= \frac{1}{S^3\alpha_3 + S^2\alpha_2 + S\alpha_1 + 1} \\
 \alpha_3 &= (C_{A1}C_{A2}C_{A3}R_1R_2R_3) \\
 \alpha_2 &= (C_{A1}C_{A3}R_1R_2 + C_{A1}C_{A3}R_1R_3 \\
 &\quad + C_{A2}C_{A3}R_1R_3 + C_{A2}C_{A3}R_2R_3) \\
 \alpha_1 &= (C_{A1}R_1 + C_{A3}R_1 + C_{A3}R_2 + C_{A3}R_3)
 \end{aligned} \tag{9}$$

, where C_{A1} , C_{A2} , and C_{A3} are defined as $K_1C_1+K_4C_4$, $K_2C_2+K_5C_5$, and $K_3C_3+K_6C_6$, respectively.

All required resistor and capacitor values can be determined from the 3rd order butterworth function [4]. Normalized pole positions are first derived based on the assumption that the low pass filter has unit cut-off frequency, and then the actual capacitor values are calculated by using the de-normalization factor, $C/(2f_cR)$, in which f_c is the actual cut-off frequency. In this design, resistor R_1 , R_2 , and R_3 are all fixed as 10K, and the resulting capacitor values for the two different cut-off frequencies are listed in Table I.

Table 1. Capacitor values of the 3rd low-pass filter

Cut-off frequency	C_{A1} (pF)	C_{A2} (pF)	C_{A3} (pF)
1 MHz	22.2	56.4	3.2
2 MHz	11.1	28.2	1.6

In order to reduce the silicon area required for the designed low pass filter, impedance multiplication technique discussed in [5] is used. As shown in Fig.4, the

equivalent impedance seen from point A to the circuit ground is $1/g_m$, and the total impedance looking into the input (VI) is $Z+1/g_m$, in which the $1/g_m$ term can be neglected if M_8 is large enough. Because there exists a fixed $1:N$ ratio between M_8 and M_9 , the total current passing through the input is $N+1$ times of the current flowing through M_1 . Thus, if Z is a capacitor C , an effective capacitance of $(N+1)C$ can be generated at the circuit input. The multiplication factor N in this design is chosen for the best power and area compromise.

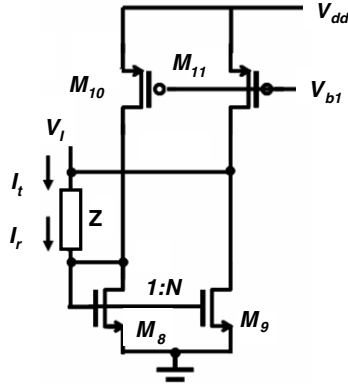


Fig. 4. Principle of impedance scaled down technique

4 Design Validation

The 3rd order butterworth low pass filter was implemented using standard CMOS 0.18 μm technology, and its functionality is fully validated under the Zeni IC design environment. Fig. 5 is the completed layout of the filter, and it occupies $250 \times 460 \mu\text{m}^2$ of silicon area.

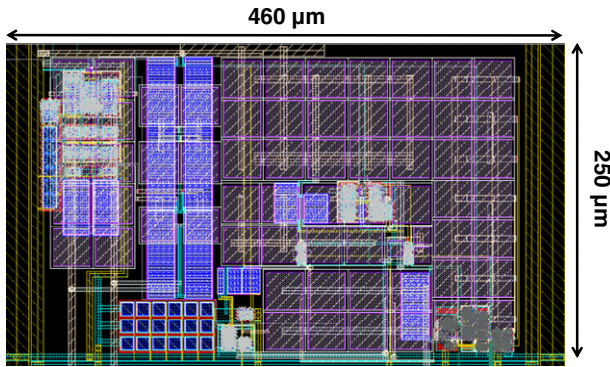


Fig. 5. Completed layout of the 3rd order butterworth low-pass filter

In order to find the proper DC bias condition to maximize the OPAMP small signal gain, under an stable bias voltage V_b , the first stage was simulated with various M_5 sizes (thus various DC bias current I_{SS}). The large signal common mode response of the OPAMP first stage with 4 different I_{SS} values (20 μA (A), 40 μA (B), 60 μA (C) and 80 μA (D)) is shown in Fig.6. Also, the common mode response of the second stage is simulated as shown in Fig.7.

For the first stage, the input common mode voltage varies from 0 to 1.8 V (Fig. 6). Complied with the theoretical analysis as shown in (3), as V_{in} increases from 0 V, the output voltage V_I decreases, until V_{in} reaches 0.6 V. Under this condition, all transistors of the first OPAMP stage enter the saturation region and V_I becomes stable. With I_{SS} varying from 20 to 80 μA , a range of stable V_I from 1.1 to 1.3 V can be achieved.

Fig.7 demonstrates that the second stage can only provide small signal gain when its input voltage, in this case V_I , is around 1.2 V, and the corresponding I_{SS} is about 40 μA .

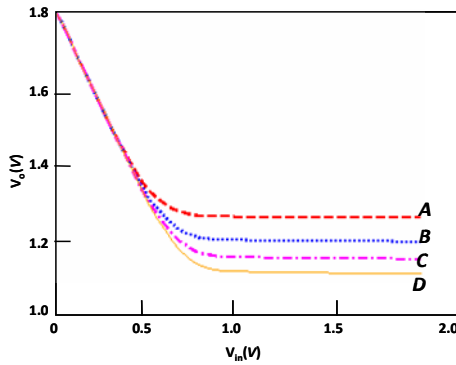


Fig. 6. Layout of the low-pass filter

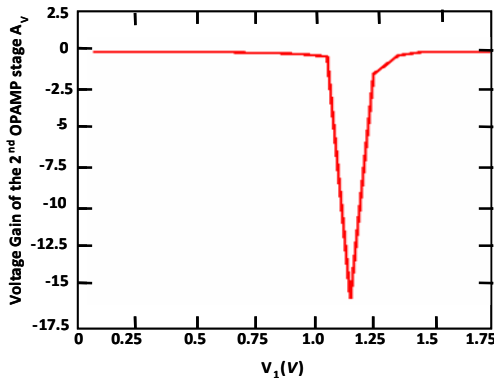


Fig. 7. Gain of the second OPAMP stage

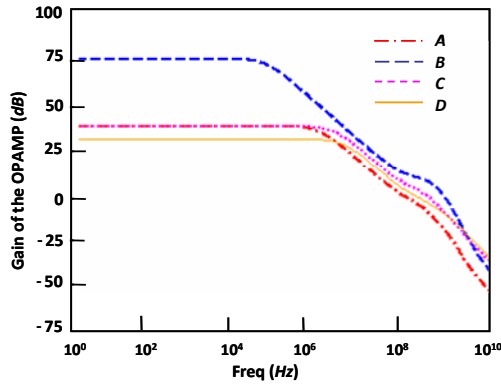


Fig. 8. AC small signal gain of the OPAMP

The response of the completed OPAMP in the frequency domain was estimated through AC simulation, and its gain with the 4 different bias current I_{SS} is plotted in Fig.8. Clearly, only when I_{SS} is set to 40 μ A and V_1 is about 1.2 V, the OPAMP can achieve high gain. The simulated DC gain of the OPAMP in this bias condition is about 80 dB, and the 3-dB bandwidth is about 75 kHz.

The completed 3rd order butterworth low-pass filter was also characterized, and the gain and phase responses are given in Fig.9 and Fig.10. In the figures, curve E and F represents the cases when the filter cut-off frequency is set to 1 MHz and 2 MHz, respectively. The completed filter has 0 dB insertion loss, and the overall power consumption is only 200 μ W with a stable 1.8 V power supply.

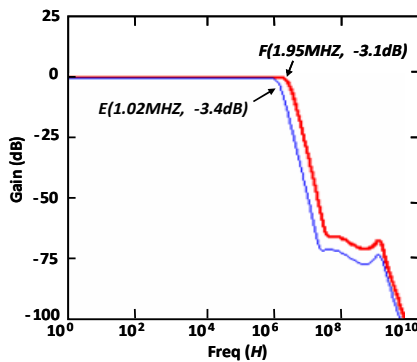


Fig. 9. Gain of the completed low pass filter

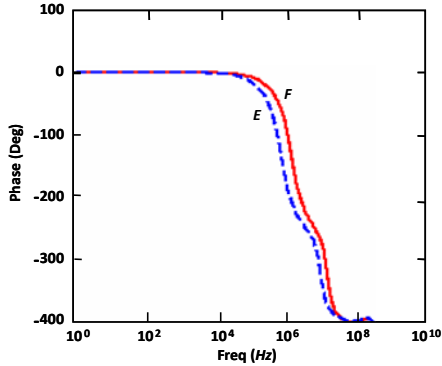


Fig. 10. Phase of the completed low pass filter

5 Conclusion

A 3rd order butterworth low-pass filter with tunable pass-band designed for the 5.8 GHz receiver is presented in this paper. The filter is based on a single two-stage OPAMP, and the tunability is achieved by digital-controlled capacitor array. The filter was implemented in standard CMOS 0.18 μm technology, and was fully characterized under the Zeni IC design environment. Simulation results show that the completed filter has 0 dB insertion loss, with configurable bandwidth of 1 MHz or 2 MHz, while consumes only 200 μW from a 1.8 V power supply.

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