Development of a MIMO/OFDM-Based Gbps Wireless Testbed for IMT-Advanced Technologies

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Abstract. According to International Telecommunication Union (ITU) requirements, future IMT-Advanced systems should support peak data rates of 100 Mbps and 1 Gbps, respectively, in high-speed mobile environment and stationary/pedestrian environment. In order to achieve this goal and evaluate related wireless technologies, we develop a MIMO/OFDM-based TDD-mode Gbps wireless testbed. This article describes the design details of its system architecture, frame structure, transmitter and receiver structures. Four types of broadband multimedia applications are used in system experiments and performance demonstrations in real indoor environments. With an effective transmission bandwidth of 96.48 MHz, our wireless testbed can achieve more than 1 Gbps transmission data rate with good Bit Error Rate (BER) and Frame Loss Rate (FLR) performance in stationary environments for different high-layer multimedia applications.

Keywords: IMT-Advanced, Wireless Testbed.

1 Introduction

International Telecommunication Union (ITU) is currently promoting the research and standardization of IMT-Advanced mobile systems, which set some key benchmarks for the development of next generation mobile communication systems. Specifically, in ITU-R recommendation M.1645 [1], future IMT-Advanced systems can support peak data rates of 100 Mbps and 1 Gbps, respectively, in high-speed mobile environment (up to 350 km/h) and stationary/pedestrian environment (up to 10 km/h), with scalable transmission bandwidth varying from 20 MHz to 100 MHz.

In order to achieve this peak data rate of 1 Gbps, many leading telecom companies have put a lot of effort in researching and developing advanced wireless testing platforms with IMT-Advanced characteristics. In December 2004, Siemens claimed that they had tested 1 Gbps wireless transmission in real time, by using Orthogonal Frequency Division Multiplexing (OFDM) technique and an intelligent antenna system consisting of three transmitting and four receiving antennas. A 100 MHz band in the unlicensed 5 GHz frequency range was used in this experiment. In May 2005, DoCoMo achieved 1 Gbps data rate over 101.5 MHz radio transmission bandwidth by

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implementing a 4-by-4 multiple-input-multiple-output (MIMO) antenna system in a field experiment [2]. In addition, a MIMO wireless system employing eight transmitting and eight receiving antennas was developed in 2006 by Electronics and Telecommunications Research Institute (ETRI), Korea, to support Gbps data transmissions [3].

Funded by the Ministry of Science and Technology (MOST) of China under the 863 high-tech program and FuTURE research projects, several leading universities and research institutions in China have started to do research on Beyond 3G (B3G) mobile systems since 2003 [4]. In 2006, a prototype B3G system was demonstrated and tested in a multi-cell mobile environment in downtown Shanghai. A peak data rate of 100 Mbps was achieved by using a novel Generalized Multi-Carrier transmission technique [5]. Recently, the National Mobile Communications Research Laboratory at Southeast University has been working closely with Huawei Technologies to develop an advanced wireless testbed with 1 Gbps transmission data rate. Different from previous demo systems, this Gbps wireless testbed aims to test, evaluate and demonstrate some key transmission technologies and broadband multimedia applications for future IMT-Advanced mobile systems.

This article first describes the system architecture of this Gbps wireless testbed, its hardware platform, frame structure, transmitter and receiver structures, key functions and modules, some implementation issues and the corresponding technical solutions. Several experiments with a variety of data-centric broadband applications are then conducted in different indoor environments to evaluate and demonstrate system capability and performance of this wireless testbed for IMT-Advanced technologies. Finally, a few research topics for future work are discussed.

2 System Architecture

Our Gbps wireless testbed consists of one transmitter and one receiver. They have the same hardware platform, but can be configured into a Base Station (BS) and a User Equipment (UE), respectively, by using programmable logics and Software Defined Radio (SDR) technology. As shown in Fig. 1, the hardware platform for the transmitter/receiver includes three parts: (1) Digital Baseband Signal Processing (DBSP) subsystem, (2) Intermediate Radio Frequency Signal Processing (IRFSP) subsystem, and (3) RF processing subsystem.

DBSP subsystem consists of one control board and two Digital Signal Processing (DSP) boards, which are installed in an industry standard chassis with over 20 Gbps interconnecting data throughput between the slots. Each DSP board is equipped with six Xilinx XC5VSX240T FPGA devices, an embedded MPU controller, a Gigabit Ethernet (GE) switching device, DDR memory devices, etc. The whole DBSP subsystem provides 12 digital optical fiber interfaces (blue boxes in Fig. 1) and two GE interfaces (red boxes in Fig. 1).

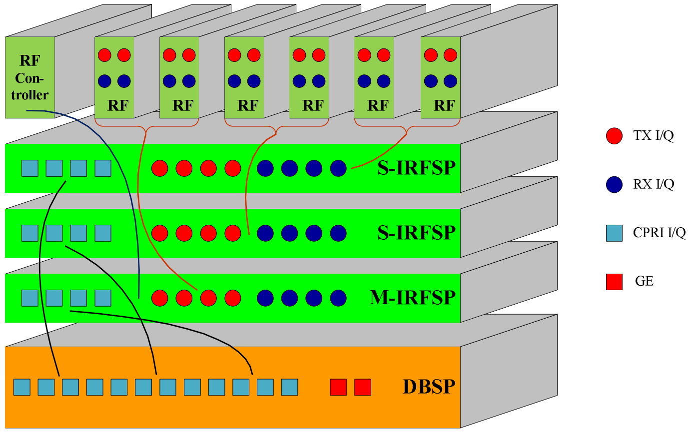


Fig. 1. System Architecture of Hardware Platform

IRFSP subsystem consists of a Master IRFSP (M-IRFSP) module and two Slave IRFSP (S-IRFSP) modules, each module corresponds to two RF antenna channels and has four digital optical fiber interfaces and four pairs of interfaces for transmitting (red circles in Fig. 1) and receiving (blue circles in Fig. 1) differential analog signals to and from RF processing subsystem. By using the high-speed serial signal transmission protocol of the Common Public Radio Interface (CPRI) industry standard, a maximum transmission data rate of 3.072 Gbps can be achieved through 12 digital optical fibers between DBSP and IRFSP subsystems.

RF subsystem consists of six RF processing modules, corresponding to six antennas and their analog signal processing units. Each antenna has I and Q orthogonal signal transmission channels, so each RF module has two pairs of interfaces for transmitting and receiving differential analog signals. IRFSP and RF subsystems are connected by shielded coaxial cables and parallel data cables for transmitting and receiving I/Q orthogonal analog signals, reference clock signal, and RF control information (from M-IRFSP module to RF control unit).

3 Module Design

Our Gbps wireless testbed adopts MIMO technology and OFDM modulation (1024-point FFT) in both uplink and downlink transmissions, with four transmitting antennas and six receiving antennas. In total, 1024 subcarriers (numbered from 0 to 1023) can be supported and each has a bandwidth of 120 KHz. Among them, 800 subcarriers (i.e. {2,…, 401; 622,…, 1021}) are employed for effective data transmission and 4 unused/virtual subcarriers (i.e. {0,1,1022,1023}, near zero frequency band) are assigned for improving system performance after carrier suppression, thus the total transmission bandwidth is equal to 96.48 MHz. A total number of 768 effective subcarriers are used for carrying data symbols from user applications. Pilot symbols are carried by the remaining 32 effective subcarriers, which are uniformly distributed across the entire frequency band for data transmission.

3.1 Frame Structure

We choose Time Division Duplex (TDD) mode for developing this Gbps wireless testbed. As shown in Fig. 2, the length of a frame is defined as 5ms. Each frame consists of a downlink subframe and an uplink subframe, corresponding to physical downlink and uplink transmission channels, respectively. A downlink subframe contains a downlink Preamble (one OFDM symbol, 9.375 μs) and several time slots (nine in Fig. 2) for downlink data transmissions. Similarly, an uplink subframe contains an uplink Preamble and several time slots (one in Fig. 2) for uplink data transmissions. Downlink and uplink subframes are separated by Downlink to Uplink Switching Point (DUSP) and Uplink to Downlink Switching Point (UDSP), which have a length of 53.125 μs. In TDD mode, the allocation of downlink and uplink time slots can be dynamically adjusted according to the instantaneous data rate requirements from upper layer user applications. The length of a time slot is 487.5 μs, which includes one Midamble (two OFDM symbols), one control word (one OFDM symbol), and 49 OFDM data symbols.

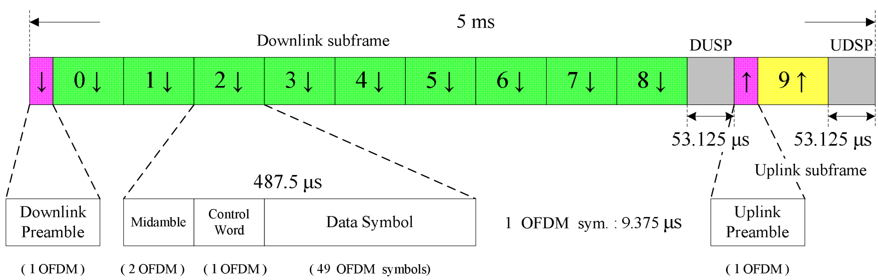


Fig. 2. Frame Structure

Both downlink and uplink subframes start with a Preamble, which has the same duration as an OFDM symbol and is used for time synchronization and frequency offset estimation at receiver side. A Preamble consists of a Cyclic Prefix (CP) of 1.042 μs and a preamble training sequence of 8.333 μs, which is constructed by using Golay complementary sequences and satisfies two requirements: (1) it has a good (sharp) time-domain correlation function, and (2) its frequency-domain transformed sequence is simple, thus it is easier to develop a differential sequence for assisting frequency offset estimation.

A Midamble with the length of two OFDM symbols is assigned at the beginning of each time slot, which is a 400-point Zadoff-Chu training sequence used for a receiver to measure and estimate Channel State Information (CSI) in current time slot. The following control word is used to carry delay-critical control and feedback information about current communication channels.

3.2 Transmitter Structure

The transmitter structure is shown in Fig. 3. User application data first goes through a LDPC channel encoder, a bit interleaver is then applied to encoded data blocks, the output sequence is mapped into symbols by using high-order Quadrature Amplitude Modulation (QAM) schemes. After that, a multi-antenna multiplexing module splits the symbols into four independent parallel data streams, each corresponding to a transmitting antenna. On each path of an antenna, a fixed number of data symbols are combined with a Pilot training sequence before conducting Serial-to-Parallel (S/P) conversion, Inverse Fast Fourier Transform (IFFT), and P/S conversion. Next, Cyclic Prefix (CP) will be added to form data frames. At the same time, pre-defined Preamble and Midamble training symbols will be inserted according to the frame structure specified in physical layer. Finally, a multi-antenna selection module selects four antennas (out of six) for data transmissions.

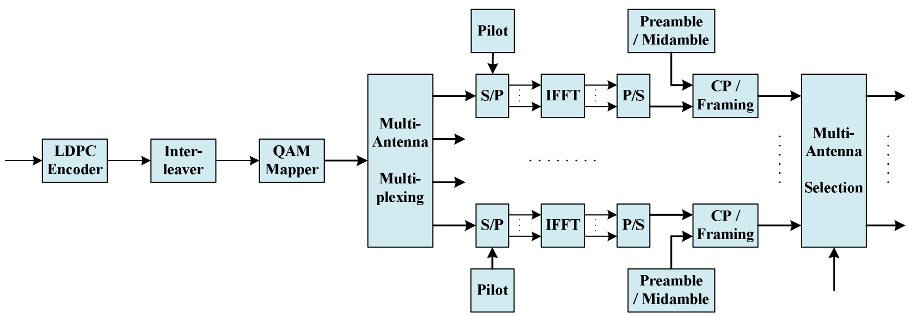


Fig. 3. Transmitter Structure

Based on the actual modulation scheme used in physical layer, the number of active transmitting antennas, and the distribution of effective subcarriers carrying application data, we develop a joint interleaving and multi-antenna multiplexing scheme to meet the following requirements:

a) adjacent coded bits should be transmitted by non-adjacent antennas,
b) adjacent coded bits should be mapped to non-adjacent points in a modulation constellation diagram,
c) adjacent coded bits should be allocated as far apart as possible to different frequency subcarriers.

Due to interleaving, multi-antenna multiplexing and IFFT functions, the signal energy of each encoded data symbol block spreads in time, space and frequency domains, thus a receiver can potentially achieve multi-domain diversity gains jointly.

Multiple transmitting antennas send the same Preamble symbols simultaneously, in order to assist a receiver quickly achieving time synchronization and frequency offset estimation. Pilot symbols are uniformly distributed across the effective transmission bandwidth, thus helping a receiver effectively estimate the residual frequency offset and phase shift. Orthogonal Midamble training sequences are sent by multiple transmitting antennas in time and frequency domains, respectively, so as to aid a receiver to estimate instantaneous CSI of current communication channels.

3.3 Receiver Structure

Fig. 4 shows the block diagram of receiver structure in our Gbps wireless testbed. As seen, the receiver has symmetric upper and lower data paths (separated by a dash line), which contain the same set of physical layer modules to conduct synchronized baseband signal processing in parallel. We use six receiving antennas, so the hardware modules in each path need to handle simultaneously the sampled baseband signals from three receiving antennas through CPRI interface. First, the receiver uses a correlation method in time domain to search Preamble symbols, thus achieving coarse time synchronization and frequency offset estimation. Fine time synchronization can be accomplished after correcting the frequency offsets in received Preamble symbols. In doing so, we can identify from the sampled sequences the starting points of S/P conversion of OFDM data symbols. Then, frequency-domain OFDM symbols can be obtained by (i) correcting the frequency offsets in time-domain data symbols, (ii) removing their CPs, and (iii) executing FFT algorithms. These OFDM symbols are from three receiving antennas (corresponding to the application data carried by 400 effective subcarriers) and need to be exchanged between upper and lower signal processing paths, so the channel estimator and MIMO multi-antenna signal detection modules in both paths will process, in parallel, only half of the frequency-domain OFDM data symbols from all six receiving antennas.

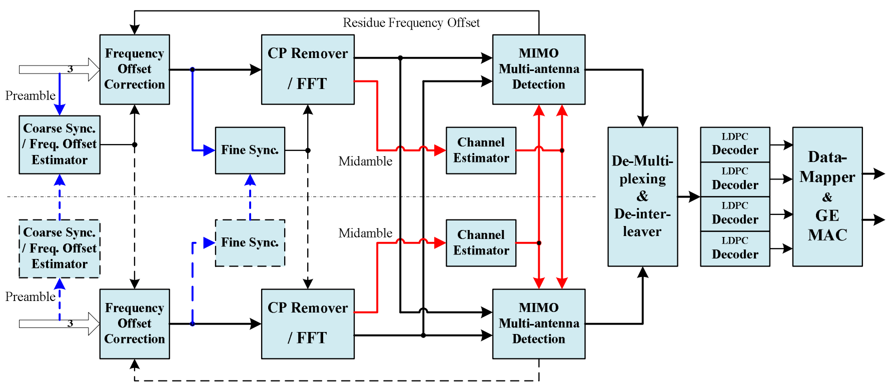


Fig. 4. Receiver Structure

The complex matrix of channel responses between multiple MIMO antennas can be estimated in frequency-domain by calculating the correlation relationship between predefined training sequences and received Midamble symbols. Specifically, a Least Squares (LS) criterion is used to estimate the frequency-domain channel responses of the subcarriers carrying Midamble training sequences, the CSI of other effective subcarriers can then be calculated by applying cubic spline interpolation or Gaussian interpolation methods [6]. A simplified Sorted QR Decomposition (SQRD) algorithm [7], which is based on the Zero-Forcing (ZF) or Minimum Mean Square Error (MMSE) criterion, is implemented for multi-antenna signal detection. Comparing to MMSE-SQRD algorithm, the baseband signal processing of ZF-SQRD algorithm is less complex in hardware implementation.

The output data symbols from two parallel MIMO multi-antenna detection modules are merged while passing through multi-antenna de-multiplexing and de-interleaving modules. In order to meet the processing-speed requirement for 1 Gbps transmission data rate, four parallel LDPC decoders are used for pipeline decoding of encoded symbol blocks. Specifically, LDPC code rate is 5/6, an encoded data block contains 12,288 bits, and a decoding algorithm with 20 iterations is used. Finally, a data mapper module will process the decoded sequences from four LDPC decoders according to the MAC protocol of Gigabit Ethernet (GE), select an output GE interface, and ensure the right order of output frame sequences.

3.4 Intermediate Radio Frequency Signal Processing Subsystem

IRFSP subsystem handles Analog/Digital (A/D) and Digital/Analog (D/A) conversions of baseband signals for MIMO multi-antenna receiving and transmitting paths, respectively. It has standard CPRI interfaces to support two-way high-speed serial data exchanges with the DBSP subsystem. Depending on the number of transmitting/receiving antennas in the wireless testbed, multiple IRFSP modules can be flexibly integrated and configured into the same IRFSP subsystem, wherein each module can support the transmitting and receiving paths and interfaces for two antennas. The sampling rate for A/D conversion is 122.88 million samples per second, which is the same as baseband clock frequency 122.88 MHz. The quantization length for each sample is set to be 11 bits.

In our Gbps wireless testbed, the Master IRFSP (M-IRFSP) module obtains the clock signal from the DBSP subsystem through its CPRI interfaces, and sends clock signals to two Slave IRFSP (S-IRFSP) modules for achieving time synchronization. In addition, M-IRFSP is responsible to provide a reference clock signal to the RF subsystem, extract dedicated RF control information from the DBSP subsystem through its CPRI interfaces, and then forward this information to the control unit of RF subsystem.

3.5 Radio Frequency Subsystem

RF subsystem also has a modular structure, each RF module handles the analog signal processing functions in both transmitting and receiving paths of one antenna. Center carrier frequency is set to be 3.45 GHz, with a processing and operation bandwidth of 100 MHz (3.4GHz ~ 3.5GHz) for transmitting/receiving circuits and Power Amplifier (PA). Intermediate Frequency (IF) for Automatic Gain Control (AGC) and transmitting/receiving signal processing is set as 1 GHz. The maximum PA output power is 23 dBm and the switching time between transmitting and receiving modes is less than 5 μs in TDD transceiver.

The control unit of RF subsystem receives a reference clock signal of 15.36 MHz from the M-IRFSP module, generates a local clock signal of 10 MHz by using a Phase-Locked Loop (PLL), and then distributes it to multiple RF processing units for synchronized operations. This control unit also interprets the RF control information from DBSP subsystem (via M-IRFSP) and executes Automatic Power Control (APC) and AGC in multiple RF transmitters and receivers, respectively.

4 Performance Evaluation and Demonstration

A series of experiments and field trials of our Gbps wireless testbed have been carried out at National Mobile Communications Research Laboratory, Southeast University, China, and Shanghai Research Center for Wireless Communications (WiCO), China, to evaluate and demonstrate its capability and point-to-point data transmission performance. Fig. 5 shows a corridor layout for our testbed experiments. The corridor is about 43 meters long and 2.4 meters high. It consists of concrete cement walls from floor to ceiling (shown in solid lines) and big glass windows to the ceiling with one-meter high concrete windowsills (shown in dash lines). The floor is covered with polishing glazed tiles, and the ceiling is metal frame plasterboard. There are seven concrete supporting pillars, represented by hatched boxes, distributed with intervals of eight or nine meters along the corridor. In this test environment, a BS and a Mobile Station (MS, or UE) are placed on each side of the corridor with a direct distance of 41 meters. The height of multiple antennas at BS and MS is fixed at 1.6 meters from the ground, as shown in Fig. 6.

Under TDD mode, frame structure is configured with nine downlink time slots and one uplink time slot, as the case in Fig. 2. The modulation scheme used in our experiments is 16-QAM. The maximum achievable downlink and uplink information bit rates are 921.6 Mbps and 102.4 Mbps[1], which correspond to physical-layer transmission data rates of 1105.92 Mbps (downlink) and 122.88 Mbps (uplink) after information bits are processed by the LDPC encoder with a coding rate of 5/6. Therefore, the summed (two-way transmissions) information bit rate and encoded data rate are 1.024 Gbps and 1.2288 Gbps, respectively. These figures are calculated after removing the time slots and frequency subcarriers allocated to Preamble, Midamble and Pilot symbols.

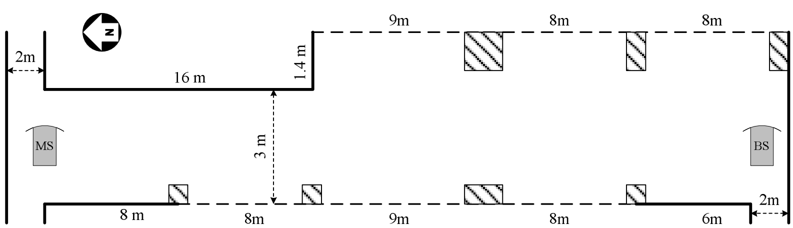


Fig. 5. Test environment

To generate Gbps-level user data traffic, four types of broadband applications are considered in the experiments and trials.

(a) Uncompressed High-Definition Television (HDTV) video streaming
(b) High-speed FTP file downloading

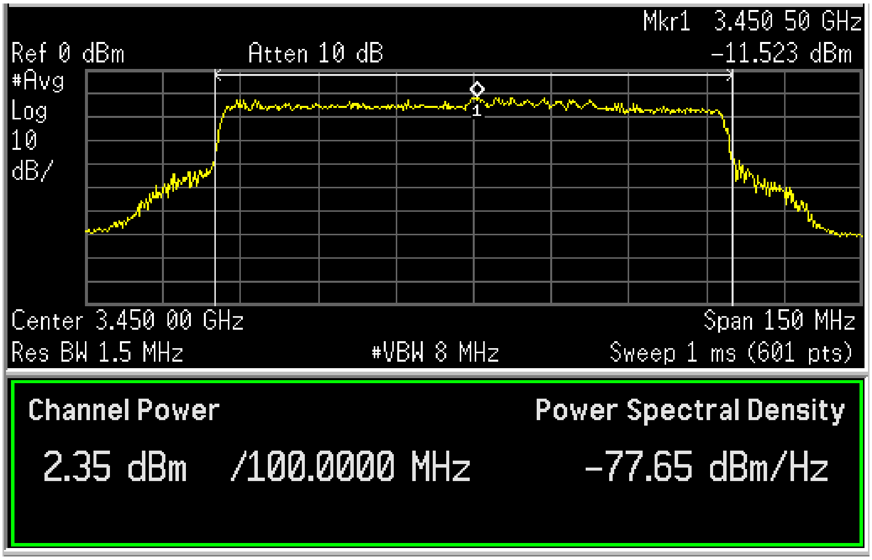
[1] In our experiments, the Control Word symbol in a frame time slot is also used for data transmission. So the information bit rate for one time slot is calculated as 102.4 Mbps = 50 (data symbols per time slot) × 5/6 (LDPC coding rate) × 4 (index for 16-QAM modulation) × 4 (number of transmitting antennas) × 768 (number of effective subcarriers for data transmission) × 200 (number of frames per second).

(c) Real-time video streaming from High-Definition Video Camera (HVC)
(d) Video On Demand (VOD) data streaming

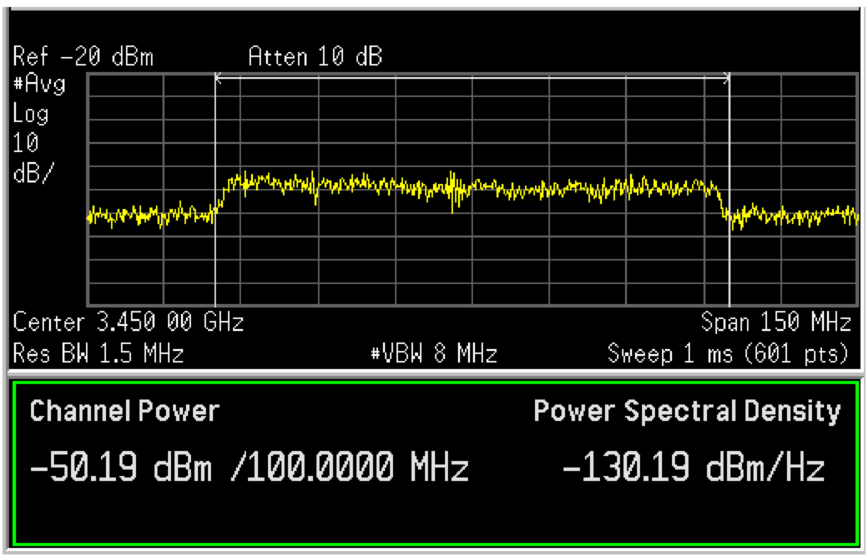
Uncompressed HDTV traffic is used only for downlink transmission, its streaming frame rate is 35 frames per second, the resolution of a video frame is 1280 × 720 pixels, 24-bit color quantization is used for each pixel, so the theoretical streaming data rate is 774 Mbps (35 × 1280 × 720 × 24). Other three applications will generate a combined traffic data rate of about 100 Mbps for both downlink and uplink transmissions. These applications are aggregated and input as Ethernet data packets (based on UDP/TCP/IP protocols) by an application server through two GE interfaces of the DBSP subsystem at transmitter (BS) or receiver (UE) side. This aggregated application traffic directly feeds into the LDPC encoder in Fig. 3. Besides, control and feedback messages of UDP, TCP and IP protocols are added to downlink and uplink data transmissions.

Fig. 6. Installation of the Gbps Wireless Testbed (one side)

As shown in Fig. 6, six MIMO antennas are linearly placed on both sides of the Gbps wireless testbed. The width and height of this antenna array are 1 meter and 1.6 meters (from the ground). Four and six antennas are used for data transmission and reception, respectively.



(a)Output Signal at a Transmitter Antenna



(b)Input Signal at a Receiver Antenna

Fig. 7. Average Channel Power at Transmitter and Receiver Antennas

When center carrier frequency, transmission bandwidth and power control word are set to be 3.45 GHz, 96.48 MHz and 6A (Hex)[2] , respectively, Fig. 7 shows the average channel powers of (a) output signal at a transmitter antenna and (b) input

[2] A step power increment of 0.5dB is specified for the transmission power control word, its maximum value “7F (Hex)” corresponds to the maximum transmission power.

signal at a receiver antenna. Considering the gains in both transmitting and receiving antennas, a power attenuation of 52.54 dB (2.35 + 50.19) is observed for wireless signals over the experimental distance (about 40 meters).

In our experiments, the received uncompressed HDTV video streaming data can be smoothly playback. According to the measurement data, the baseband Signal-to-Noise Ratio (SNR) at the receiver is about 18 dB, the output Bit Error Rate (BER) after multi-antenna detection reaches 10^{-6} level, the corresponding Frame Error Rate (FER) after LDPC decoder is less than 10^{-4}. The statistical results from video players Windows DirectX and MontiVision SDK (www.montivision.com) both demonstrate a Frame Loss Rate (FLR) less than 2×10^{-4}. At the application server, we install the traffic measurement software Bandwidth Meter Pro (www.bandwidth-meter.net) and observe (i) the average data rate of uncompressed HDTV video streaming traffic (downlink) is 748 Mbps, and (ii) the peak data rate of combined FTP file downloading and real-time HVC video streaming traffic (downlink and uplink) is 136.5 Mbps.

The above testing results are obtained in an indoor corridor environment with certain keyhole tunnel characteristics, which contain a very strong Line-of-Sight (LOS) signal component and several weak scattering signal components. Therefore, the position and spacing of multi-antenna deployment at transmitter (BS) or receiver (UE) will greatly affect the correlation relationships between MIMO channels, hence the wireless channel capacity and BER performance. In addition, we have conducted a series of experiments with the Gbps wireless testbed in an indoor environment with rich scattering signal components and a weak direct LOS signal component. In this scenario, the correlations between MIMO channels are low and wireless channel capacity is relatively high. As expected, a better BER performance is observed, which is also much more robust against multi-antenna positions and spacing, wireless interference, and random movements of people in the laboratory.

5 Conclusions

This article describes the development and evaluation of a MIMO/OFDM-based TDD-mode Gbps wireless testbed, which meets the key requirements on data transmission of future IMT-Advanced mobile systems. The design details of system architecture, frame structure, transmitter and receiver structures are presented and discussed. Four types of broadband multimedia applications are used in system experiments and performance demonstrations in real indoor environments. By adopting MIMO/OFDM techniques and an effective transmission bandwidth of 96.48 MHz, our wireless testbed can achieve more than 1 Gbps transmission data rate with good BER and FLR performance in stationary environments for different high-layer multimedia applications.

Further, we will use this wireless testbed to research, develop and evaluate some potential wireless technologies for IMT-Advanced mobile systems, such as complex channel estimation algorithm based on Linear Minimum Mean Square Error (LMMSE) criterion and Discrete Fourier Transform (DFT) interpolation method [8], Quadrant Detect and QR Decomposition based Maximum Likelihood Detection (QD-QR-MLD) algorithm for multi-antenna signal detection [9], adaptive channel coding, high-order modulation and multi-antenna multiplexing schemes based on instantaneous CSI and user QoS requirements, cross-layer optimization techniques for dynamic control of MAC protocols and network traffic parameters. In order to support wireless testing experiments in high-speed mobile environments, we can uniformly increase the number of Midamble symbols within each time slot, thus improving channel estimation performance in fast-fading channel conditions (at the expense of reduced system throughput). We will then investigate key technologies and system performance in outdoor mobile environments, and develop and evaluate effective cooperative schemes between multiple BSs in distributed antenna systems [10].

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