Phase Measurement of Three-Phase Power Based on FPGA*

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Abstract. As the frequency of the three-phase power signal is instability and it contains multiple harmonics signal, the error can not be ignored when FFT algorithm applied to measure the phase directly. Although corrected by many correction methods such as ratio method, center of energy gravity method, etc. the precision of phase measurement is also severely influenced by harmonic signal. In order to solve these problems, the power phase measurement system is designed based on FPGA which embedded all-phase FFT algorithms. It realized the measurement of the phase with high accuracy, and the results indicate it almost immune to the harmonic and noise of power.

Keywords: Phase Measurement, All-phase FFT, FPGA.

1 Introduction

The phase of three-phase voltage and current signal is one of the most important measurement issues of the power test and control system. The research on the phase of voltage and current signal focuses on how to get the accurate measurement result rapidly. As the main method of digital signal processing, FFT is often used to measure the phase of power signal. For the frequency of the three-phase power signal is instability and it contains multiple harmonics signal, the error can not be ignored when FFT algorithm is applied to measure the phase directly. Although corrected by many correction methods such as ratio method, center of energy gravity method, etc. the precision of phase measurement is also severely influenced by harmonic signal. With the phase invariability, the all-phase FFT is suitable to solve this problem. Based on all-phase FFT, the phase of the three-phase voltage and current signal can be measured accurately, and it almost immune to the harmonic and noise of power. In this paper, the three-phase voltage and current phase measurement system based on FPGA is proposed to realize the phase accurate measure by using the all-phase FFT algorithm.

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2 System Design

This paper proposes utilizing FPGA to realize all phase FFT algorithm, and using the algorithm to accomplish phase and phase difference's measure of the three-phase electricity. Due to FPGA has characteristics of design flexibility and fast processing-speed, so the phase measurements based on FPGA can be realized conveniently and also make it meet the real-time measurement requirements. Using the signal regulate circuit to convert the three-phase voltage current signal to A/D conversion chip's required range, realize High voltage signal's isolation, expand 6 road 12 bits high-speed synchronous ADC and collect three-phase voltages and three current signal simultaneously, then process the collected multiple signals in FPGA chip and calculate some measured value such as the voltage and current phase and so on. The three-phase electricity phase measuring system overall charts based on FPGA are shown in Figure 1.

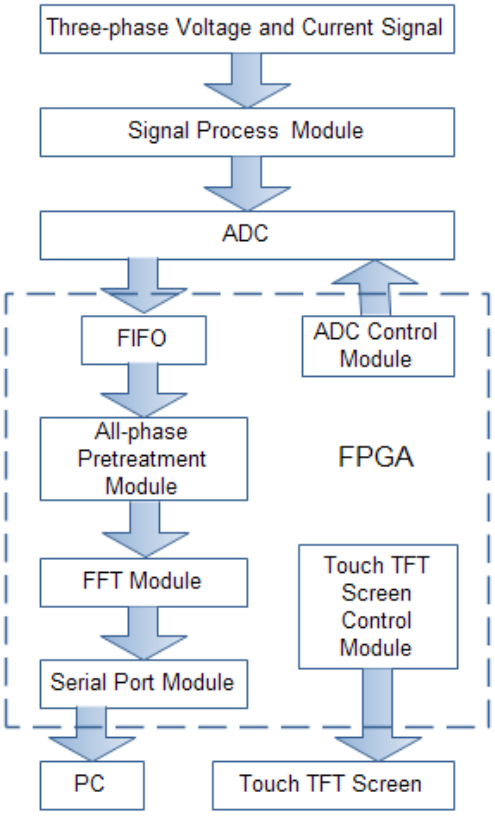

Fig. 1. The three-phase voltage and current phase measurement system framework based on FPGA (Dotted box is FPGA)

2.1 Hardware Circuit of Measurement System

(1)Voltage and current signal process module

No distortion test of three-phase electrical signals is the premise to realize phase signal's high precision measuring. Design signal regulate circuit can convert 380V ac voltage signal to the voltage signal within A/D conversion required range with no distortion, testing the input voltage to effect the A/D converter.

(2)ADC module

ADC module's sample quantization is a necessary step to realize digital signal processing. Design ADC sampling module to convert the three-phase voltage current analog signals into digital signals, and then send it to FPGA for digital signal processing.

(3) The FPGA function module

The FPGA function module is the core of the three-phase electricity phase measuring system that it not only deal with data, but also control the whole system's coordination. This module mainly responsible for collecting data on all phase pretreatment, FFT processing, cut transform and the control work of modules such as ADC, LCD, Flash Memory and so on.

(4) Touch Screen

In the design of three-phase electricity phase measuring system, touch screen realized the function of keys in order to facilitate future function expansion and upgrades. Because the touch screen coated in the upper part of the LCD display screen, so functions that can be realized in different area of the touch screen are provided by LCD modules, namely, touch screen and LCD display are used together with as buttons.

(5) PC Software

PC mainly accept the FFT frequency domain data coming from Serial, and then finish anyway, cutting operations and calculate the phase in Labview software. At last, show the user a visual interface with displaying measured results graphically.

2.2 The FPGA Function Modules

(1)Asynchronous FIFO module

Asynchronous FIFO module has two main roles, the first role is to complete ADC sampling data's receiving. ADC samples the three-phase signal under the control of FPGA, and then stores the sampled data into FPGA for processing. The second role is to complete speed matching between modules. Due to ADC chip's speed limits, the advantage of FPGA fast speed can't be fully exerted. In order to make the entire system treat operations as soon as possible, we must introduce asynchronous FIFO to solve this problem, which finishes reading and writing data operations through two separate clocks. As ADC's low speed, we can set low frequency clock to finish the writing operation of sampled data. And also because the preprocessing module needs large quantity, so we need to set higher frequency clock to finish the reading operation of data.

(2) All phase pretreatment module

All phase pretreatment module is the core of system algorithm. The phase spectrum invariability of Acquisition signal after transformed by FFT can be assured only after the signal has been all phase preprocessed. And the phase invariability is not only the premise of precision measuring, but also the suggested theoretical basis of this design. All phase pretreatment which based on FPGA is mainly use FPGA' owning eighteen bits on-time multiplier to complete the pretreatment work, thus getting the N preprocessing data. The on-time multiplier's multiplicand is the sampled data that coming from FIFO module, while the multiplier is the convolution coefficient stored in the procedure. Treat the 2N - 1 item data which get from the on-time multiplier as following: item 1 plus N + 1 item, the first 2 plus N + 2 item until the first N - 1 plus item 2N - 1 item, and then put N item before N-1 item. Finally get N point pretreatment data.

(3)FFT module

FFT module invokes Altera Company's Quartus II 9.1 software's bringing FFT IP core to finish the FFT processing. This IP nuclear processing precision can reach 24 bits in binary, and there are many structural frames to choose from. So we can be reasonable to use FPGA hardware resources to do FFT transformation quickly and efficiently. In this design, FFT used a flow pattern data structure with a fixed transform size. The input and output are continuous flow of data, and the output data format is mass index structure which is a compromise structure between designated structure and floating-point structure.

(4)Serial interface module

Serial interface module mainly be responsible for transmitting the specific FFT frequency-domain data to the PC, and also use anyway, cutting processing to find out the corresponding phase values in Labview software. The results of FFT transformation are plural, and then use its imaginary part to divide its real part. Next, this point phase value is the value of that number’s arc tangent.

(5) Control module

Control module is responsible for coordinating the whole system, such as control the ADC initialization, control the data acquisition and transmission, control the touch screen initialization and control signal transmission and so on.

3 Hardware Design

The three-phase electric measuring system based on FPGA not only should ensure the phase measuring accuracy, but also should assure the real-time measuring requirements. So the chip selection and hardware circuit design were crucial.

3.1 Features of the Chip

(1) ADC chip

ADC uses the MAXIM’s MAX1308 chip whose sampling accuracy can up to 12-bit and maximum sampling rate reaches 4Msps.Except that,it has 8 acquisition channels. Three-phase voltage and current signal data’s acquisition requires 6

channels, so the sampling rate of each channel signal can up to 600ksps, it is easy to meet requirements of the three-phase electrical phase measurement. MAX1308 chip uses 12-bit parallel port to communicate with the FPGA, which can sent the 12 bits collected data to the FPGA for processing at the same time,and also can control the FPGA' work mode by received control word coming from FPGA to make it complete tne acquisition of three signal phase.within time sequence.

(2) FPGA chip

The project selected the Altera Cyclone Ⅱ series FPGA chip EP2C35F672C8N which with a hardware multiplier inside. The chip is the core of the phase measurement system which not only processes the data, but also controls the entire system's work coordination. The main responsibility of this chip includes doing all preprocessing phase to the collected data, FFT processing, data operations,and ADC, LCD, Flash etc. chip's control work. Due to FPGA chip having the feature of thirty-five 18-bit multiplier that not only guarantees the speed of all preprocessing phase、FFT processing and the arctangent computation, but also will not take up too much hardware resources.

(3) Touch screen and LCD display

TSC2046 of Texas Instruments Company is selected to be used in this project. This chip can test the press points on the two-dimensional screen, and it's highest detection accuracy can up to 12 bits. LCD display is a LCD color display with a size of 3.0 inches,and resolution of 400×240 pixel. Between the LCD display and FPGA chip is connected the control chip ILI9326of Technology Company which used to drive the LCD display and can show 65K colors (18 bits).

3.2 Design and Working Principle

(1) Regulate circuit design

The phase measuring systems based FPGA can not detecte the 380V three-phase electrical signals directly,while it is necessary to design the signal regulate circuit to convert the AC voltage with amplitude of 380V to the required range of ADC samples with no distortion. Secondly, in order to ensure detection of phase with no distortion and the original phase information not changed in the process of the regulate circuit convertion. We used the principle of resistance's partial voltage in the design for the resistance won't make the signal phase information lead or lag.

(2) Sample circuit design

In design of the phase measuring system ,the design of sample circuit is very critical and it's Stand or fall has a direct impact on the accuracy of the measuring results.As the Three-phase electricity has three-phase voltage and three-phase current ,so when measure it's phase value simultaneously,it required at least 6 ADC acquisition channels. MAX1308 chip of MAXIM company has 8 acquisition channels, and it's sampling accuracy can up to 12-bit ,maximum sampling rate reaches 4Msps The three-phase voltage and current signal's data acquisition requires 6 channels, so the sampling rate of each channel signal can up to 600ksps, it is easy to meet requirements of the three-phase electrical phase measurement. The MAX1308 chip uses dual power to supply and 12-bit parallel port to communicate with the FPGA,That is to say, we can sent 12 bits collected data to the FPGA for processing at

the same time,and also, MAX1308 chip can control the FPGA's acquisition channels by the 8-bit control word of FPGA.

The input high voltage of MAX1308 chip's digital port neeeds at least 0.7 times the DVCC. When the DVCC selects 5V, the high voltage which FPGA output to the MAX1308 will not be recognized.So DVCC should choose 3.3V Digital Power. If selecting external clock, R3 is always be connected to it . On the contrary,R4 would be connected to it.

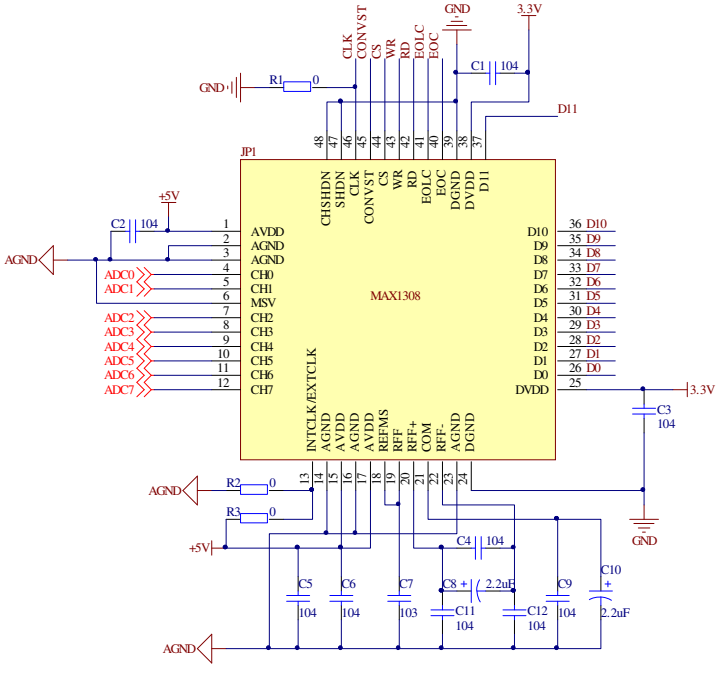

Fig. 2. Sampling circuit

4 Software Design

4.1 The Platform of Software Design

The software development platform of the design is used Quartus II. Quartus II is a comprehensive PLD developing software of Altera Company. It supports various design input forms such as Principle Diagram, VHDL, Verilog HDL, AHDL (Altera Hardware Description Language) and so on. What's more,it has embedded integrated device and emulator, and can complete the PLD design flow from design input to the hardware configuration. Quartus II supports Altera's IP Core which contains Macro function module base of LPM/Mega Function. So the users can use the mature module fully, simplify complexity of the design and accelerate it's speed. The good

support for third-party EDA tools also allows the user to use the familiar third-party EDA tools in all stages of the design process.

The hardware design language is VHDL, which is a high-level language used in circuit design. VHDL is mainly used to describe digital system's structure ,behavior, function and interface. The design ideas based on the VHDL state machine is especially embodiment in this design. State machine can be thought as a special combination of portfolio logic and registers logic. Portfolio logic part can be divided into state machine decoder and output decoder, and state decoder determines the next state of the state machine. Output decoder determines the state machine's output.

4.2 Program Design

(1) Acquisition procedures

Acquisition procedures is the control program of MAX1308 chip. The key problem of the control program is to ensure the points of each acquisition from began gathering to end integer times the FFT needed points, in order to ensure that each FFT have effectively output. In this design, state machine thought is adopted to complete the data acquisition control. Programming design flow chart as Figure 3 shows.

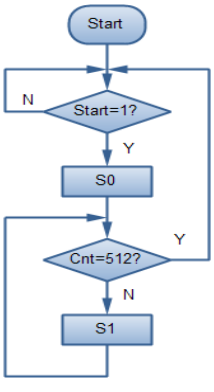

Fig. 3. Data acquisition flow chart

On the right flowcharting, S0 represents initialization state of MAX308,S1 represents a state of waveform sampling,Start represents start collecting signal, Cnt is collecting counter.

From reading the picture,we know even if the Start becomes 0 in sampling, the acquisition circulation won't be affected. And it will not stop until 512 data bits collected. When start collecting, the MAX1308 should be initialized and its acquisition channel number should be settled every time. The collection timing diagram of Quartus II simulation is as shown in Figure 4.

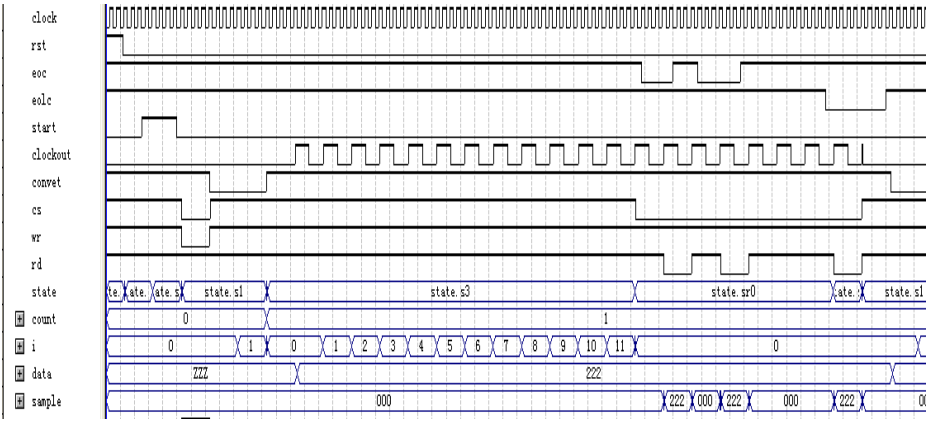

Fig. 4. Collection timing diagram

(2) FFT program

Because the Quartus II supports Altera's IP core,which curing various modules such as Adder module, Multiplication module, division module, FFT module, FIFO module and so on.So the design invokes the IP core's FFT module to reliaze it's own FFT. The FFT is taking advantage of the flow pattern data structure, transform size is 64 (take fewer points facilitate simulation and validate the results). The FFT results of Quartus II simulation is shown in Figure 5.

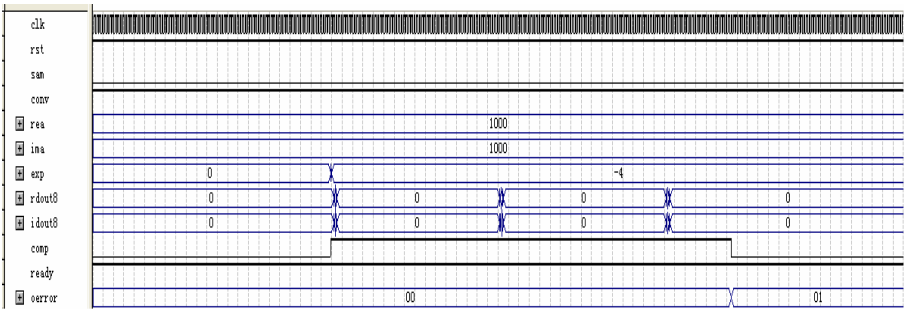

Fig. 5. Simulation timing diagram

As the above figure shows, if the real part and imaginary part input are 1000, the first item of FFT transformation result is 64000 and other items are 0.And rea, ima in the charts are Separately referred to the real part , imaginary input. Exp, rdout, idout are Separately referred to the quick exponential term, the real part ,imaginary part output. According to the handbook of FFT's IP core, we can get to know the final output is rdout*2(-exp) and idout*2(-exp).

(3) Touch screen control module procedure

The touch screen's control procedure mainly contains correct control of TSC2046 chip and ILI9326 chip. The TSC2046 chip must receive and transit data bidirectionally

with the FPGA chip,while the ILI9326 chip only need to receive the control information and the data message correctly from the FPGA chip. In the design ,we discovered that as these two chips must transmis information with the main chip frequently and high-speedly,therefore the timing control becomes very important and we must eliminate the competition risk which possibly appears in the procedure as far as possible. This module's timing chart is as shown in Figure 6. DIN first outputs control word of the Y coordinate, and then outputs control word of the X coordinate.

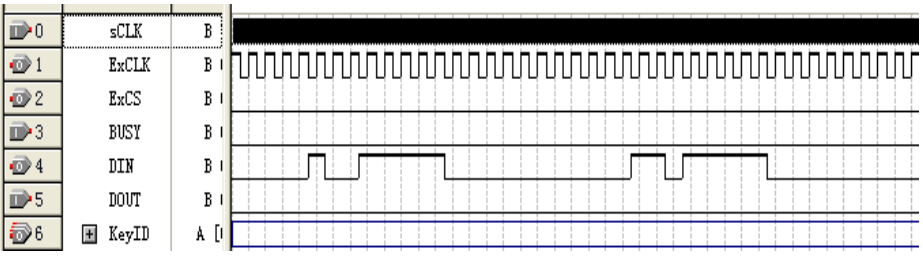

Fig. 6. Touch screen control timing diagram

5 System Commissioning

5.1 Hardware Circuit Debugging

This design is a extending system based on EP2C35F672C8N chip's teaching and multimedia development platform,and that the EP2C35F672C8N chip belongs to Altera company's Cyclone Ⅱ series. In the three-phase electricity phase detection system, the first thing is to design special voltage regulate circuit, which can convert the three-phase 380V power distortionless into the range of high voltage signals,which ADC conversion required.As there are three voltage signal road in the three-phase electricity, So if we want to measure the instantaneous phase difference between each phase,there must have multiple acquisition channel in the acquisition circuit to ensure synchronous sampling and transform the three-phase voltage current analog signals into digital signals. Then, use a FPGA to make a full phase FFT processing to the transmited ssion digital signal.Finally,translate the data to PC through serial port and use Labview software to test and verify them.

5.2 Practical Measurement Based on Labview

Combining Labview with acquisition card can validate all phase FFT phase detection algorithm. Use the acquisition card which controlled by FPGA to collect and process three-phase electricity, and then send the data though serial data bus to PC and display them on the Labview software. Finally, the measured results are shown in Figure 7.

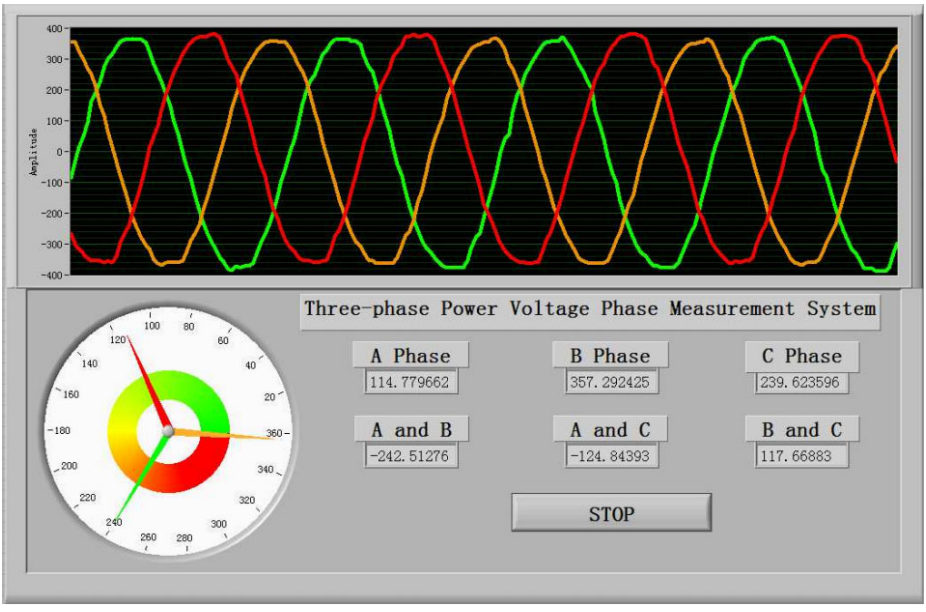

Fig. 7. Phase detection interface of Labview

6 Summary

This system design all phase FFT algorithm based on FPGA, which phase invariability makes it does not acquire any compensation algorithm correction to calculate three-phase electricity phase values. Realize the overall design of three-phase electricity phase detection system, and measured its phase value with a higher precision and practical value. All that laid a foundation for the further three-phase electricity phase measurement special chip (ASIC)'s research.

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