# A Comparative Study of Placement of Processor on Silicon and Thermal Analysis

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**Abstract.** Today when we have stepped into the second decade of this century, the integrated circuits are getting more and more complex with multicore processors. With technology scaling, more devices are being integrated into a small area. As a result, heat dissipation in integrated circuits (ICs) has increased. The processor is one of the highest heat generating components in an IC. The temperature generated in an integrated circuit varies with factors like number of processors, processor modes, their dimensions and arrangement on Silicon. In this paper we are presenting two simulation results. First one was obtained by analyzing how the area occupied by processor affects the temperature distribution. This study is extremely important as the area occupied by processors scales down with technology. The second study was to find out how the processor location and modes can affect temperature distribution in multicore processors. The processors at 2.4GHz frequency were analyzed in both active and idle modes. The highest and lowest temperatures and the location of hotspot in each case were analyzed.

**Keywords:** Floorplan, Hotspot, Peak Temperature, Simulation, Through Silicon Via.

## 1 Introduction

The processor architects spend considerable time in analysing the thermal behavior of various circuits. The temperature developed in an integrated circuit mainly depends on floorplan and power consumed by individual devices or units. A floorplan is the way in which the devices are arranged on the Silicon surface. Hotspot is the simulator that gives the temperature developed in each of the individual units by taking floorplan and power values as input. Its advantages are ease of use and computational efficiency. In this paper we present the results of our experiments in two phases to find the location and the value of the maximum temperature developed. The location of maximum temperature is called hotspot. In the first phase, we carried out two sets of experiments considering only a single processor to analyze how the temperature is affected by varying the area occupied by the processor on Silicon surface. The first set of experiments were carried out by considering the processor in active mode and the second set of experiments were carried out by considering the processor in idle mode. In the second phase, we did experiments with varying number of processors each with

N. Meghanathan et al. (Eds.): CCSIT 2012, Part II, LNICST 85, pp. 654–662, 2012.
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equal dimensions. The experiments were carried out with different processor modes and position on Silicon surface and temperature was analyzed.

# 2 Experimental Phase 1

In the first phase, ten experiments were carried out with a single processor to study the affect of area of processor in different modes on temperature values. The processor in the active mode consumed 50.9W power and that in the idle mode consumed a power of 13.7W.

## 2.1 Silicon Area versus Temperature Simulations Experimental Setup

A square shaped Silicon substrate with width 0.016m was taken. In the first experiment, a processor in active mode occupied the entire Silicon surface. A processor in the idle mode occupied the entire Silicon area in the second experiment. In the third and fourth experiments, the entire area of Silicon was divided into two equal sized units, each with width 0.016m and height 0.008m. The processor occupied one of these units and the other unit was vacant. Here the area occupied by processor was reduced to half of that in the first and second experiments. The processor in the third experiment was in active mode and the one in the fourth experiment was in idle mode. The entire Silicon area was divided into four identical units each with width and height 0.008m in the fifth and sixth experiments. The processor occupied one of these units and all the other three units were vacant. All the odd numbered experiments were carried out with active processor and even numbered experiments were carried out with the processor in idle mode. In the seventh and eighth experiments, the entire Silicon area was divided into eight equal sized units. The processor occupied only one by eighth of the total Silicon area. The remaining seven units were vacant. Each unit had a height of 0.008m and a width of 0.004m. In the last two experiments, the entire Silicon area was divided into sixteen equal sized units, each with a width of 0.004m and height of 0.004m. Among these units, fifteen were vacant and the processor occupied only a single unit. The details of first phase experiment are given in table 1.

**Table 1.** Details of the first phase experiments

| Experiment No: | Total Si area ($m^2$) | Area occupied by processor ($m^2$) | Processor mode | Lowest temperature (K) | Highest temperature (K) |
|---|---|---|---|---|---|
| 1 | .000256 | .000256 | Active | 326.23 | 327.66 |
| 2 | .000256 | .000256 | Idle | 320.32 | 320.71 |
| 3 | .000256 | .000128 | Active | 323.94 | 330.05 |
| 4 | .000256 | .000128 | Idle | 319.71 | 321.35 |
| 5 | .000256 | .000064 | Active | 323.52 | 334.36 |
| 6 | .000256 | .000064 | Idle | 319.6 | 322.51 |
| 7 | .000256 | .000032 | Active | 323.33 | 341.45 |

**Table 1.** (*Continued*)

| 8 | .000256 | .000032 | Idle | 319.54 | 324.42 |
|---|---|---|---|---|---|
| 9 | .000256 | .000016 | Active | 323.19 | 354.96 |
| 10 | .000256 | .000016 | Idle | 319.51 | 328.06 |

## 2.2 Temperature Profile

The temperature profile obtained in the first phase is shown in the Fig. 1. The deep red color represents the hotspot and the dark blue region represents the coolest region. As the temperature increases the color gradually changes in the order dark blue, light blue, green, yellow, orange and finally red. In all the ten experiments, the hotspot was developed in the unit in which the processor was present.

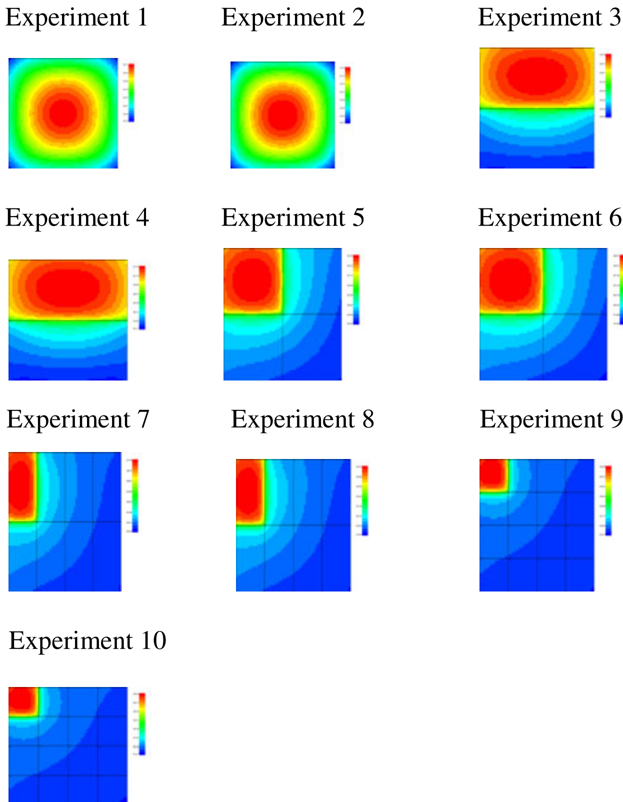


**Fig. 1.** The thermal profile of phase 1 experiments

## 2.3 Result Analysis

The temperatures obtained in the first phase have been plotted in the following four graphs. The x-axis shows the processor area in square meters and the y-axis shows the

temperature in degree Kelvin. Fig.2 shows the comparison of active and idle mode temperatures and fig. 3 shows the comparison of the highest and the lowest temperatures.

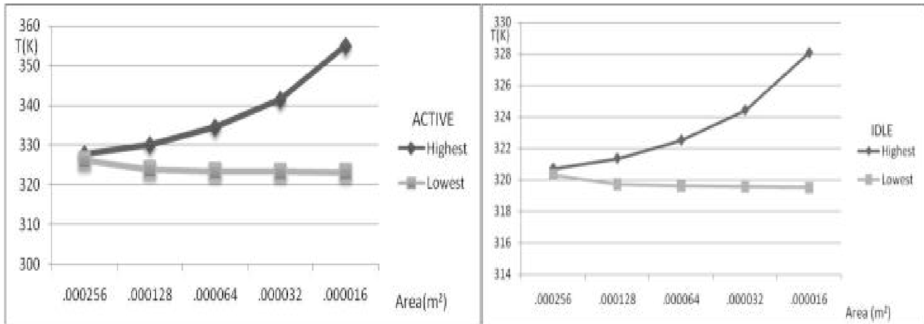


**Fig. 2.** The comparison of active and idle mode temperatures

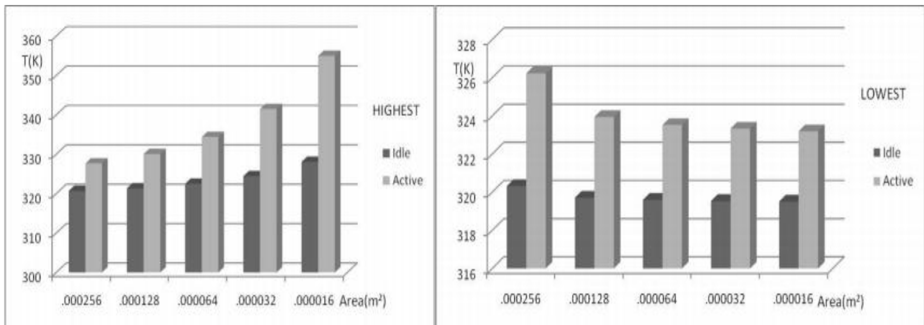


**Fig. 3.** The comparison of highest and lowest temperatures

# 3 Experiment Phase 2 Setup

The phase two was an extension of the experiments5 and 6 of phase 1. Here also a square shaped Silicon substrate with width 0.016m was taken. The entire silicon area was divided into four identical units in the floorplan with width 0.008m and height 0.008m. The number of processors, their location and modes varied in each experiment. The processor in the active mode consumed 50.9W power and that in the idle mode consumed a power of 13.7W.

## 3.1 Processor Placement Simulations

In the second phase, sixteen experiments were carried out. The first six experiments were carried out using two processors. The next four experiments were carried out using three processors and the final six experiments had four processors. The floorplans for each of the sixteen experiments is as shown in fig.4. The arrangements of the processors can be better understood from the table 2.

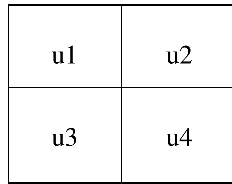


**Fig. 4.** The floorplan in the second phase experiments

**Table 2.** The arrangement of processors in second phase

| Experiment No: | Total number of processors | u1 | u2 | u3 | u4 |
|---|---|---|---|---|---|
| 1 | 2 | 1 idle processor | 1 idle processor | vacant | vacant |
| 2 | 2 | 1 idle processor | 1 active processor | vacant | vacant |
| 3 | 2 | 1 active processor | 1 active processor | vacant | vacant |
| 4 | 2 | 1 idle processor | vacant | vacant | 1 idle processor |
| 5 | 2 | 1 idle processor | vacant | vacant | 1 active processor |
| 6 | 2 | 1 active processor | vacant | vacant | 1 active processor |
| 7 | 3 | 1 idle processor | 1 idle processor | 1 idle processor | vacant |
| 8 | 3 | 1 idle processor | 1 idle processor | 1 active processor | vacant |
| 9 | 3 | 1 active processor | 1 active processor | 1 idle processor | vacant |
| 10 | 3 | 1 active processor | 1 active processor | 1 active processor | vacant |
| 11 | 4 | 1 idle processor | 1 idle processor | 1 idle processor | 1 idle processor |
| 12 | 4 | 1 idle processor | 1 idle processor | 1 idle processor | 1 active processor |
| 13 | 4 | 1 idle processor | 1 active processor | 1 idle processor | 1 active processor |
| 14 | 4 | 1 idle processor | 1 active processor | 1 active processor | 1 idle processor |
| 15 | 4 | 1 idle processor | 1 active processor | 1 active processor | 1 active processor |
| 16 | 4 | 1 active processor | 1 active processor | 1 active processor | 1 active processor |

### 3.2 Temperature Profile and Result Analysis

The temperature profile of all the 16 experiments in second phase is shown in fig. 5. Here also the deep red color represents the hotspot and the dark blue region represents the coolest region. As the temperature increases a gradual change in the color of the profile from blue to red can be noted.

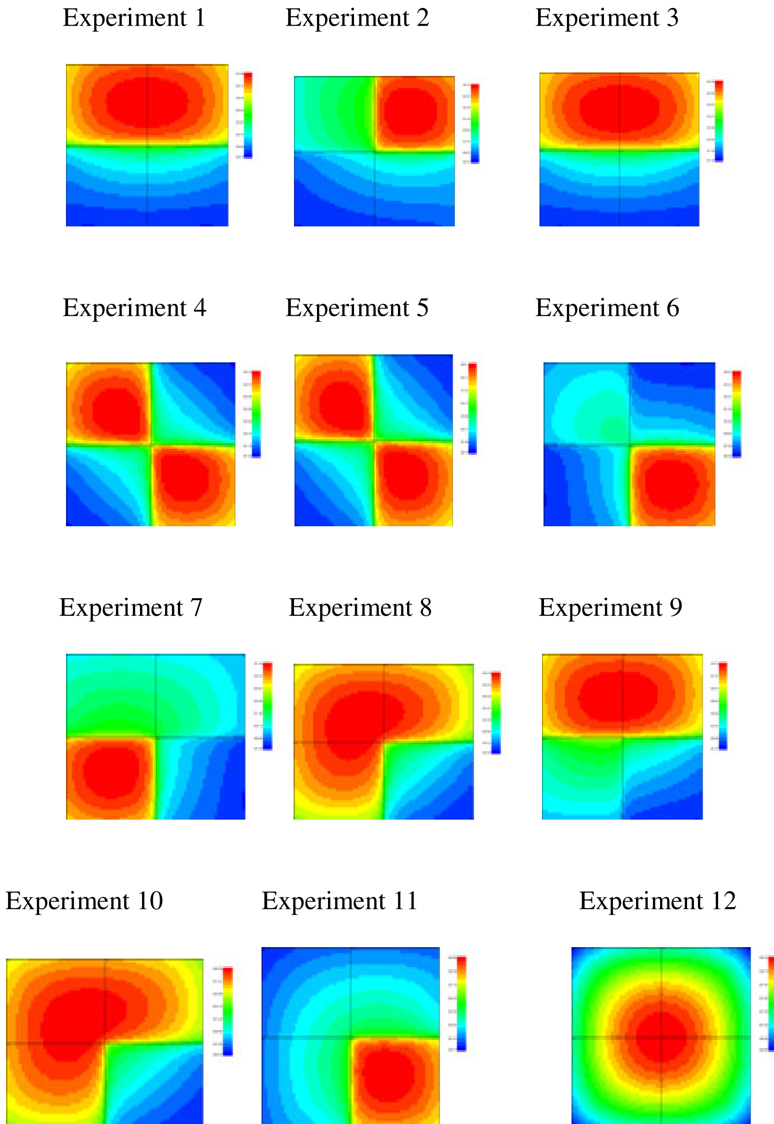


**Fig. 5.** The thermal profile obtained in phase2

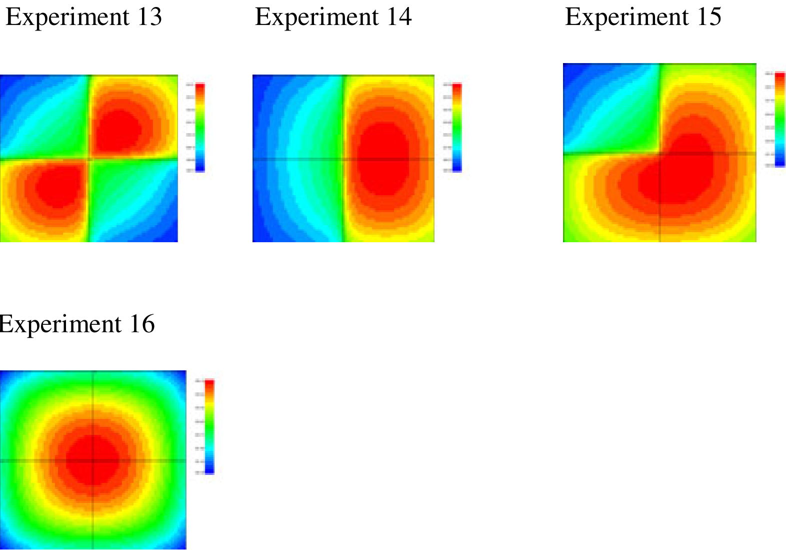


**Fig. 5.** (*Continued*)

The experiments with similar thermal profile are experiments 1 & 3, experiments 4 & 6, experiments 7 & 10 and experiments 11 & 16. The lowest and highest temperature values obtained in each of the sixteen experiments is given in table 3. The peak temperature value obtained in experiment6 was slightly lesser than experiment3. Similarly, the peak temperature value obtained in experiment4 was slightly lesser than experiment1 and that in experiment14 was slightly lesser than experiment13.

**Table 3.** Analysis of the second phase experiments

| Experiment No: | Lowest Temperature (K) | Highest Temperature (K) | Hotspot Location |
|---|---|---|---|
| 1 | 321.26 | 324.56 | Equally distributed in u1 and u2 |
| 2 | 325.21 | 336.27 | u2 |
| 3 | 329.72 | 341.96 | Equally distributed in u1 and u2 |
| 4 | 321.53 | 324.19 | u1 and u4 |
| 5 | 326.04 | 336.01 | u4 |
| 6 | 330.70 | 340.60 | u1 and u4 |
| 7 | 322.97 | 326.44 | u1, u2 and u3. Major portion in u1 |
| 8 | 327.52 | 337.94 | u3 |
| 9 | 331.47 | 343.76 | u1and u2 with majority in u1 |

**Table 3.** (*Continued*)

| | | | |
|---|---|---|---|
| 10 | 336.07 | 348.95 | u1, u2 and u3. Major portion in u1 |
| 11 | 326.84 | 328.39 | At the centre of the entire Silicon area |
| 12 | 330.77 | 339.86 | u4 |
| 13 | 335.35 | 345.56 | Equally distributed in u2 and u4 |
| 14 | 336.01 | 344.60 | Equally distributed in u2 and u3 |
| 15 | 339.94 | 350.80 | u1,u2 and u3. Major portion in u4 |
| 16 | 350.45 | 356.19 | At the centre of the entire Silicon area |

## 4 Conclusion

In all the ten experiments of phase1 hotspot was located in the centre of the processor. The lowest temperature value obtained remained almost constant both in idle and active modes when the area of the processor was reduced after the initial change. But in both the modes the highest temperature value continued to increase with decrease in area. When the area of the idle processor was reduced to one by sixteenth of the initial value the peak temperature increased by 7.35 degree Kelvin. For the processor in active mode, the peak temperature increased by 27.3 degree Kelvin when the area was reduced to one by sixteenth.This is about 3.7 times the peak temperature rise in idle mode. In phase 2 experiments, the lowest temperature was noticed in the first case that is two idle processors lying adjacent to each other. By arranging the processors diagonally opposite to each other the hotspot temperature is reduced. In all the experiments involving active processors, the entire region or a portion of hotspot was associated with active processor. The experiments with same processor number and location but different modes had similar thermal profile. But those which were conducted using active processors generated more heat.

## 5 Future Work

We will extend our experiments to three dimensional (3D) ICs. The temperature analysis will become more complex in three dimensional circuits. We will be concentrating more on a thermal aware floorplan for 3D structures. A thermal aware floorplan will reduce the peak temperature values in the different layers of such circuits. Then we will work on Through Silicon Via (TSV) modeling and thermal management solutions for 3D integrated circuits.

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