CNT Based Channel Interconnect for CMOS Devices

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Abstract. MOSFET device dimensions and dimensions of interconnects have been scaled down to increase density, functionality and performance of a chip. Recently, scaling down of dimensions, that has now reached to the nano regime, have led to various issues like electromigration as in the case of interconnects and hot carrier effects, drain induced barrier lowering and so on in case of MOSFET's. Researchers are thus trying to find other options for interconnects and also new architectures to replace the conventional MOSFET's. This paper is a study of Carbon Nanotube which is gaining interest of researchers both as device interconnect and channel-interconnect. The behavior of CNT with length and diameter is considered. A study of various parameters like mobility, conductance etc. of the CNT is done. This paper focuses on CNT based FET's, that are gaining interest as replacements for conventional CMOS, in many modern circuits and also new devices.

Keywords: CNT, CNFET, HSPICE, simulation.

1 Introduction: Carbon Nanotubes

Carbon is known to form two stable allotropes- diamond and graphite. Sumio Iijima discovered fullerene-related carbon nanotubes in 1991. Carbon nanotubes (CNTs) are cylindrical carbon molecules with outstanding mechanical, electrical, thermal, and chemical properties. The chemical bonding of carbon nanotubes is composed entirely of sp2 bonds, similar to those of graphite. These bonds, which are stronger than the sp3 bonds found in alkanes, provide nanotubes with their unique strength and they naturally align themselves into ropes held together by Van der Waals forces.

The structure of a CNT can be conceptualized by wrapping a one-atom-thick layer of graphite (or graphene) into a seamless cylinder. CNTs are of two types, namely, single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes (MWCNTs). Depending on the direction in which they are rolled (called chirality), a CNT can be semiconducting with a distinct band gap or it can be metallic with no band gap. The relationship between n and m (i.e. direction in which they are rolled) defines three categories of CNTs- metallic, semiconductive and chiral. The bending of C-C bond will introduce stress and thereby affecting the electrical properties. Metallic CNT's are being used in interconnects, both local and global and could also be used in 3D integrated circuits. Semiconductive CNT's are gaining application as channel interconnects. CNT

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based FET's i.e. CNFET's make use of the ballistic transport mechanism that is confined to the CNT channel and thereby reduce many of the short channel effects.

1.1 Ballistic Transport and Phonon Scattering in CNT

Ballistic transport is the transport of electrons in a medium with negligible electrical resistivity that occurs due to scattering. In general, the resistivity exists because an electron, while moving inside a medium, is scattered by defects, or by the atoms/molecules composing the medium that simply oscillate around their equilibrium position. The electron within its mean free path exhibits ballistic transport. Ballistic transport is observed when the mean free path of the electron is (much) bigger than the size of the medium that contains/delimits the medium through which the electron travels, such that the electron alters its motion only by hitting against the walls.

The term phonon refers to a special type of vibrational motion in which lattice uniformly oscillates at some frequency. In case of solids having different elements or bond strength between atoms, the phonon vibrations are of two types- optical phonons and acoustic phonons. Thus there are two types of scattering based on phonon i.e. acoustic phonon scattering (near-elastic) and optical phonon scattering (inelastic). The mean free path in case of optical phonon scattering is around 15nm and that for acoustic phonon scattering is around 150nm. The effective phonon scattering will be combination of both optical and acoustic phonon scattering. The scattering, both elastic scattering and phonon scattering contributes towards the resistivity in case of CNT.

2 Interconnects: Issues in Nano-Regime

The interconnect in an integrated circuit distributes clock and other signals as well as provides power or ground to various circuits on a chip. The International Technology Roadmap for Semiconductors (ITRS) emphasizes the high speed transmission needs of the chip as the driver for future interconnects development. The challenges in interconnect technology arise from both material requirements and difficulties in processing. The susceptibility of common interconnect metals to electromigration at high current densities (10^6 A/cm^2) is a problem. The electrical resistivity of Cu increases with a decrease in dimensions due to electron surface scattering and grain-boundary scattering. Such size effects arise from interface roughness and small grain size, which are hard to overcome.

Along with lower thermal conductivity and increasing current density demands from small dimension interconnects, the rising Cu resistivity also poses a reliability concern due to Joule heating that induces significant metal temperature rise. The large metal temperature rise exponentially degrades interconnect electro migration (EM) lifetime and severely limits the maximum current carrying capacity of future Cu interconnects. Also copper interconnects require lots of drivers for satisfactory performance. As an effect of grain boundary scattering, surface scattering and

background scattering, the total resistivity of Cu wire will increase. This increase in resistivity will create issues with the current conductivity and also delay.

Table 1. [13]: Minimum density of SWCNT required for exceeding the minimum Cu wire conductivity (ITRS 2010)

Technology year	2009	2010	2011	2012	2013	2014
MPU/ASIC metal 1 $^{1}/_{2}$ pitch(nm)	54	45	38	32	27	24
Cu effective resistivity(μΩ-cm)	3.8	4.08	4.3	4.53	4.83	5.2
Minimum density(nm^{-2}) for SWCNT	0.188	0.175	0.166	0.158	0.148	0.138

On the processing side, creating high aspect ratio contacts with straight walls is an extremely difficult task. Plasma damage and cleaning of high aspect ratio features also pose concerns. Void-free filling of high aspect ratio features is an equally difficult task.

3 CNT as Interconnects

CNT's are considered to be possible replacements for Cu wires as interconnects. CNTs which are a few nanometer long have better conductivity than Cu wire. The electronic transport in metallic SWCNTs and MWCNTs occurs ballistically over long lengths owing to their nearly one dimensional electronic structure. This enables nanotubes to carry high currents with negligible heating.

Although the current-carrying capacity of an isolated CNT is much greater than that of Cu, it has a high resistance (theoretical minimum of 6.45 kΩ [7], [8]). In practice, the observed resistance of an individual CNT can be much higher [8], [9], due to the presence of imperfect metal–nanotube contacts. The high resistance of an individual CNT necessitates the use of a bundle (rope) of CNTs conducting current in parallel to form a low-resistance interconnect. While MWCNT bundles are easier to fabricate, dense metallic SWCNT bundles have greater advantages in terms of interconnect performance.

Effect Of CNT Length. For lengths greater than mean free path of electron in CNT (1μm) scattering will be more. This causes decrease in electrical conductance (Fig 1 (a)) and drift velocity (Fig 1(d)). Thermal conductance (Fig 1(b)) decreases with length while propagation delay (Fig 1(c)) will increase.

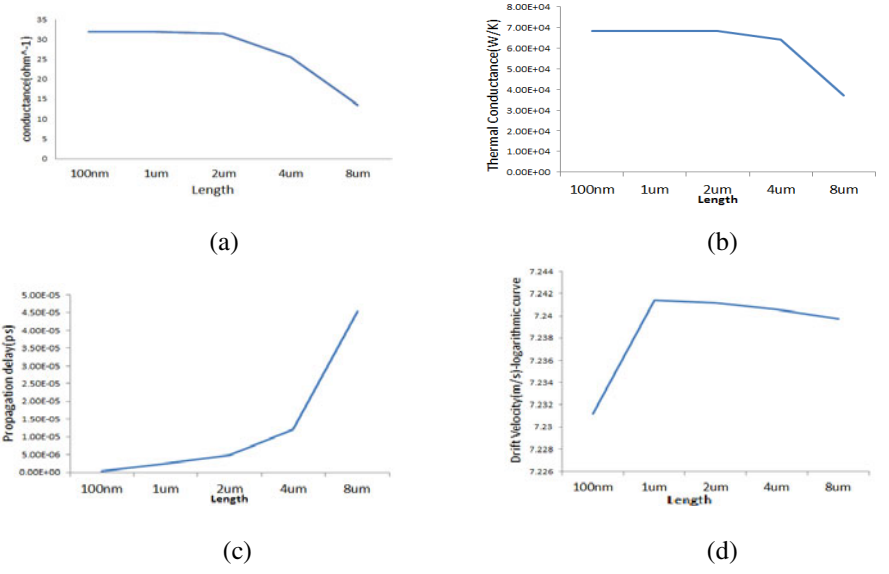


Fig. 1. [14]: (a) Electric conductance (b) Thermal conductance (c) Propagation delay and (d) Drift Velocity for Bundled CNT's as a function of length

Field Effect Mobility. The field effect mobility will increase with the length of the CNT and beyond 1μm it attains saturation. The saturation mobility is dependent on the charge density of the CNT. Lower the charge density higher will be the saturation mobility. The field effect mobility of CNT's will increase with diameter of the CNT. For higher charge densities the mobility will decrease for same diameter of CNT.

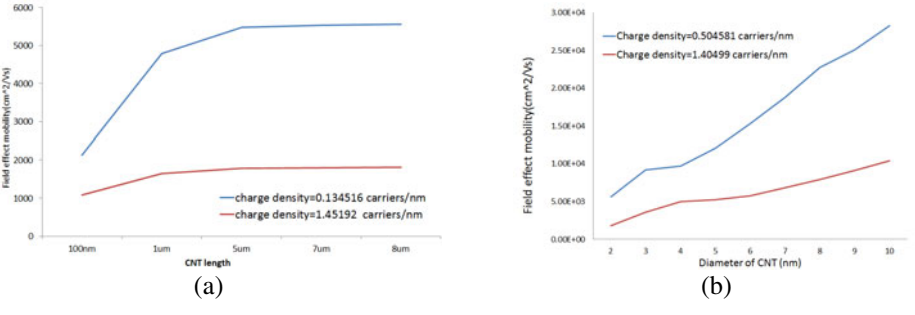
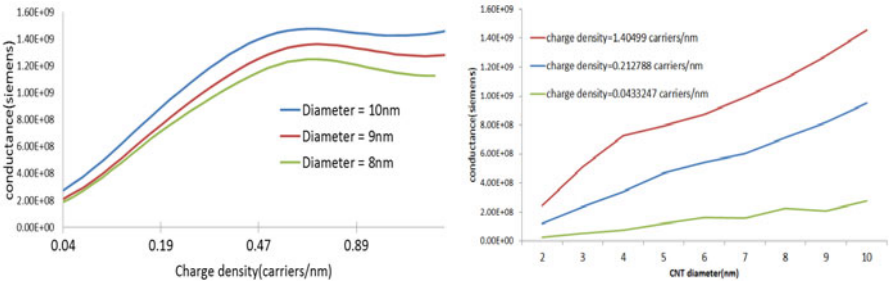


Fig. 2. [14]:(a)Field effect mobility with CNT length and (b) FE mobility with CNT diameter

Conductance. Conductance will increase with charge density of the CNT but will reach saturation at higher charge densities. This can be extended by increasing the diameter of the CNT. As seen from Fig 3(b) for same charge density the conductance will be higher for larger diameter CNT's.



(a) (b)

Fig. 3. [14]: (a)Conductance Vs. charge density for different CNT diameter and (b) variation of conductance with CNT diameter

4 Carbon Nanotubes as Channel Interconnect

Carbon nanotubes (CNTs) and carbon nanotube field effect transistors (CNFETs) have demonstrated extraordinary properties and are widely accepted as the building blocks of next generation VLSI circuits. Various structures making use of CNT's are under study or development, such as Cylindrical CNFET, Schottky barrier CNFET, Single gated CNFET, Double gated CNFET, etc.

Carbon-nanotube field-effect transistor (CNFET) avoids most of the fundamental limitations for traditional silicon MOSFETs. With ultra-long (~1 μm) mean free path (MFP) for elastic scattering, a ballistic or near-ballistic transport can be obtained with an intrinsic carbon nanotube (CNT) under low voltage bias.

In planar CNFET, parallel semiconducting CNTs are grown on or transferred to a substrate. The regions of CNTs under the gate are undoped. The conductivity of these undoped regions is controlled by the gate. The source and drain regions of the CNTs are heavily doped. The gate, source and drain contacts, and interconnects are defined by conventional lithography.

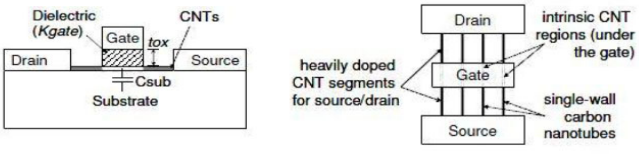


Fig. 4. [3]: Carbon –Nanotube Field Effect Transistor (CNFET)

The CNFET consists of contacts, p+ doped source and drain regions of semiconducting CNTs for PFET or n+ doped source and drain regions of semiconducting CNTs for NFET and undoped or intrinsic regions of CNTs under the gates. The distances between gates and contacts are limited by the lithographic feature size. Since CNTs are grown on the substrate, the inter-CNT distance is not limited by lithography. Multiple carbon nanotubes are allowed under the same gate (i.e. multiple tubes per device). The CNTs at the ends observe less charge screening effects than those in the middle.

4.1 Study Based on HSPICE Model of CNFET

A general study based on HSPICE model of CNFET [3][4] is done. The drain characteristics are similar to that of MOSFETs. From the obtained gate characteristics we can see that the current becomes saturated at high gate voltages. Applying higher gate voltage will not further increase the current through the CNFET channel i.e. the CNT. The point of saturation can be extended by applying higher drain to source voltage.

Applying gate voltage will cause more electrons to accumulate in the CNT channel. By applying more gate voltage more number of electrons will be pumped into the CNT. High drain to source voltage can pull these electrons and cause more current to flow. In case of lower Vds, the flow of electrons is slow and the current will be saturated at lower gate voltages itself.

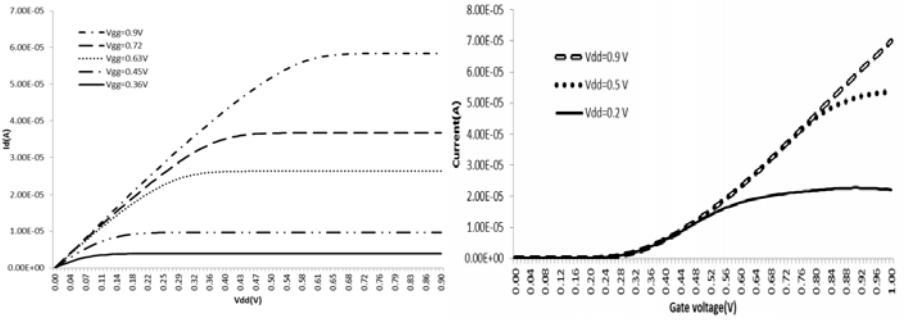
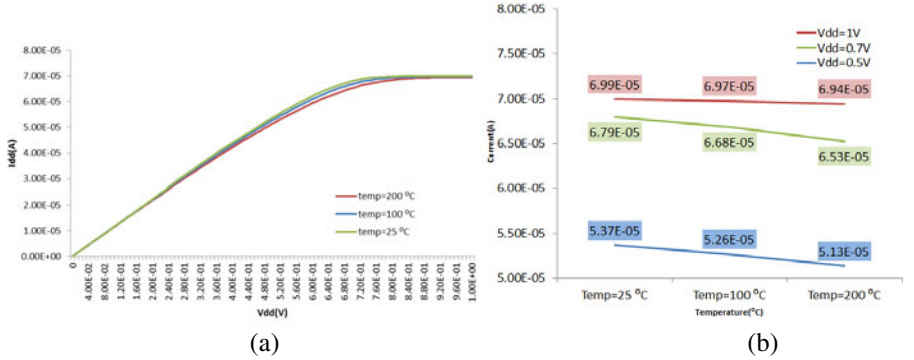


Fig. 5. Drain current Vs Drain Voltage and Drain current Vs Gate voltage

Effect of Temperature. When the temperature increases there is a decrease in the current through the CNFET. This can be considered due to the increase in the resistance. From the slope of the Drain current Vs drain voltage(Idd Vs Vdd) curve, the resistance for CNFET is found to increase with temperature.



(a) (b)

Fig. 6. Drain current for different temperature

Table 2. Increase in resistance of CNFET with increase in temperature

Temperature(^{o}C)	25 ^{o}C	100 ^{o}C	200 ^{o}C
Resistance(Ω)	9.572K Ω	9.77K Ω	10.045K Ω

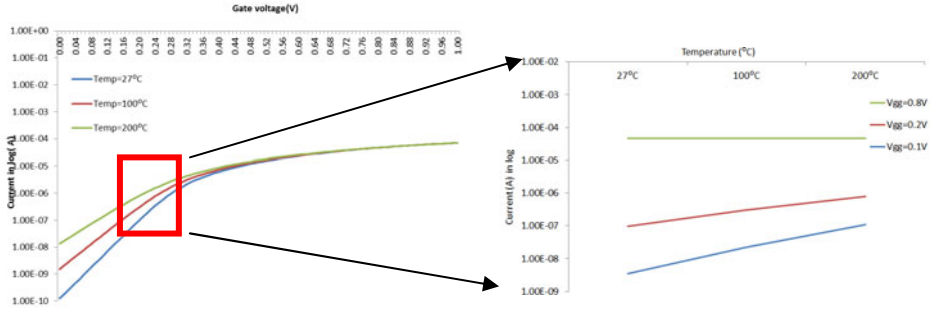


Fig. 7. Current observed when varying the gate voltage for different temperatures

The effect of increase in temperature (Fig 7), is more for low gate voltages(Vgg=0.1V) than higher gate voltages(Vgs=0.8V). Increase in temperature increases the subthreshold current through the CNFET.

Table 3. Increase in subthreshold current with temperature

Temperature(^{o}C)	25 ^{o}C	100 ^{o}C	200 ^{o}C
Subthreshold current(A)	2.87E-08	1.938E-07	9.5E-07

The current through the CNFET increases with increase in temperature for same gate voltage. Threshold voltage shows a decrease as the temperature increases(Fig 8).

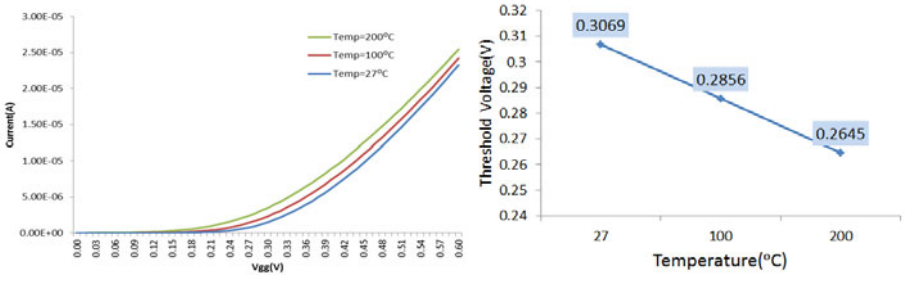


Fig. 8. Effect of temperature on threshold

Effect of Channel Length. The current though CNFET will increase as we go on increasing the length of CNT channel, as long as the scattering effects are negligible. For same voltage the current through the given CNFET is higher for longer channel CNFET (Fig 9).

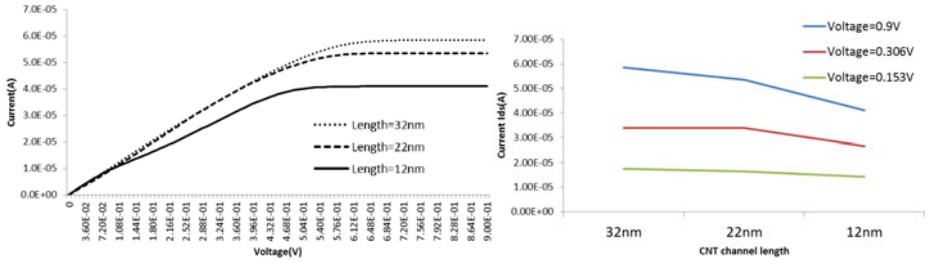


Fig. 9. Effect of channel length of CNFET on current

Gate Oxide Thickness. The thickness of gate oxide is an important parameter. In nanoscale devices, a high k dielectric is used that has high breakdown electric field and also prevents injection of electrons into the gate region. The current increases as we decrease the gate oxide thickness (Fig 10). As the gate oxide thickness is reduced, voltage drop across oxide is less and more voltage is available over the CNT channel, thereby increasing the effect of gate voltage control and more electrons are pumped into the CNT channel.

As in the case of MOSFET's, when the thickness of gate oxide is reduced ,low gate voltage is required to turn on the device and thus for lower gate oxide thickness we have lower threshold device (Fig 11). Threshold voltage for CNFET with 10nm gate oxide thickness is around 0.4V while for the oxide thickness of 1nm the threshold voltage reduces to 0.35V.

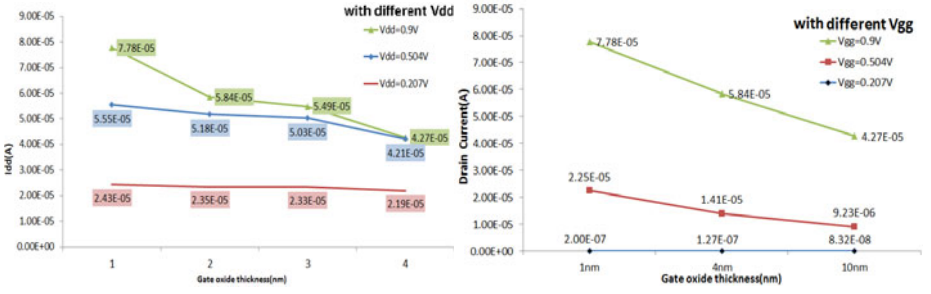


Fig. 10. Variation of current with the gate oxide thickness

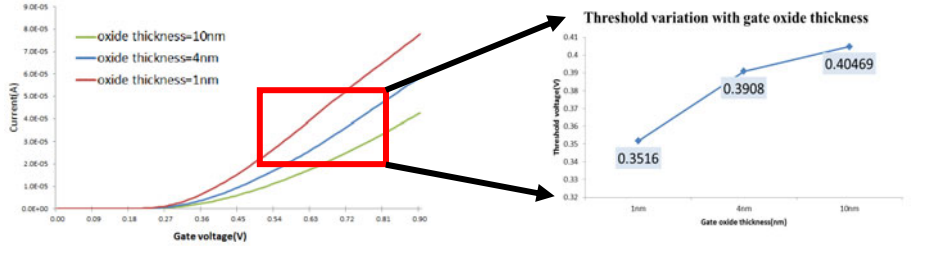


Fig. 11. Threshold variation with the gate oxide thickness

Subthreshold Current. Beyond the threshold, the current increases linearly with the applied gate voltage (Fig. 12). In the subthreshold region, which is less than 0.2V here, the current increases exponentially. CNT based FET's have got significant subthreshold current as per the given CNFET model. Calculated subthreshold current from Fig 12. is 3.82E-08A. This shows that even in subthreshold region the CNFET has high current. So they can be also used in devices operating in subthreshold region.

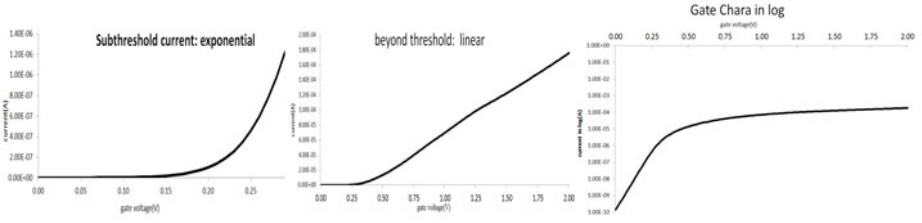


Fig. 12. The current in subthreshold, beyond threshold region and in log scale

Number of CNT's and Type of CNT used in Channel. There is not much change in current when the width of the gate region is increased (Fig. 13(a))as most of the current flows through the CNT itself. So if we increase the number of CNT channels, an increase in current is observed (Fig.13(b)). As for MOSFET, gate width also plays a major role in the amount of current through the channel. Metallic CNT have higher current than the chiral type CNT, while semiconductive type CNT has lowest current (Fig.13(d)).

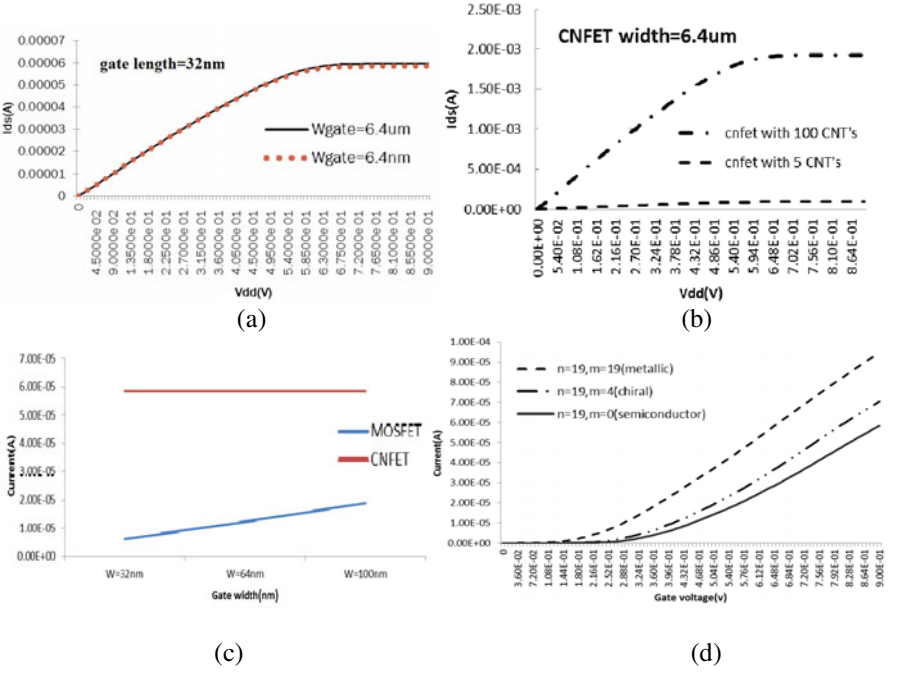


Fig. 13. Effect on current for (a) different channel width and (b) number channels (c) comparison of MOSFET AND CNFET current with gate width and (d) for different types of CNT channels

5 Conclusion

Depending upon the chirality, there are metallic and semiconducting CNT's. Metallic CNT's find application as interconnect materials. Semiconducting CNT's are used as channel interconnects in MOSFETs. The conduction process through the CNT is ballistic transport mechanism under the condition that the channel length is kept comparable to the mean free path (~1um). CNT's have got inherent resistance against electromigration and have high thermal conductivity and electrical current density.

Electrical conductance of CNT's decreases and propagation delay increases with increase in CNT length. It is also observed that drift velocity will increase till the mean free path of electron in CNT. Beyond the mean free path length, the drift velocity decrease due to scattering. Single walled and multi walled CNT and their bundles are used for interconnect applications.

CNT's are used as channel interconnects in FET's. The CNT can be placed between two doped regions that act as source and drain or can be made to have Schottky contact (metal–semiconductor contact). A study based on HSPICE model for CNFET was done. As per the model, the drain characteristics where found similar to the MOSFET while current reaches saturation for higher gate voltages while keeping the drain to source voltage constant. This current saturation at higher gate voltages can be extended by increasing Vdd. The current in subthreshold region is found to be exponentially increasing while the current beyond subthreshold is increasing linearly. There is variation of threshold with temperature and also with gate oxide thickness. These properties are similar to the MOSFETs. It was observed that the current through CNTFET remains same when the gate width is reduced keeping the channel length constant, while in the case of MOSFET the gate width also have significant contribution in current. To increase the current through the CNFET the number of CNT channels are to be increased. Significant amount of subthreshold current is present in CNFET. CNFET's can be used in low voltage applications. The amount of current and also the subthreshold current can be reduced by reducing the number of CNT's in the channel.

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