Qualitative Optimization of Coupling Parasitics and Driver Width in Global VLSI Interconnects

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Abstract. Analyses of the effects of interconnect wires in deep sub-micron technology is of prime importance in the modern era integrated circuits. The performance parameters such as crosstalk noise and delay are fundamentally dependent on interconnects and driver sizing. The coupling parasitics are the primary source of crosstalk. This paper addresses the optimization of coupling parasitics and driver sizing qualitatively for delay and peak noise. For this study, a pair of distributed *RLC* lines each of 4mm length is considered. These lines are coupled inductively and capacitively. The SPICE waveforms are generated at far end of lines for varying coupling parasitics and width of aggressor driver PMOS while keeping channel width of NMOS half of PMOS. The simulation is carried out at 0.13µm, 1.5 V technology node. Both the cases of simultaneous switching of inputs *i.e* in-phase and out-of-phase are taken into consideration.

Keywords: Delay, Crosstalk noise, Coupling parasitics, Driver width, Optimization.

1 Introduction

During the last two decades, the level of integration has increased mainly due to rapid progress in processing and interconnects technology [1]. The higher performance and improvement in circuit density has been mainly achieved by scaling down the device dimensions. Scaling device dimensions below 0.2µm resulted large consumption of chip area for complex interconnects. Thus, with technology advancement, interconnects have turned out to be more and more important than the transistor resource. According to International Technology Roadmap for Semiconductors (ITRS) [2], the gap between interconnection delay and gate delay will increase to 9:1 at 65nm technology node and on-chip wire length is expected to increase to 2.22 km/cm^2 by the year 2010. Thus, for high speed high density chips, it is mostly the interconnections rather than the device performance that determines the chip performance [3], [4].

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The use of low resistance material, faster signal rise time, longer wire length and high switching speed leads to significant value of line inductance [5]. Due to the presence of wire parasitics, the *RLC* distributed model or transmission line model is more effective in current technology [6], [7]. In addition to wire parasitics, interwire or coupling parasitics *i.e.* mutual inductance (M) and coupling capacitance (C_C) have significant value in the circuit because of short spacing between interconnects, long wire lengths, high frequency of operation and complex geometry. The value of mutual inductance between two lines depends on the value of inductance of each line, their separation, the strength of current and its rate of change. The coupling capacitance is limited to adjacent neighbors and to adjacent layers in multilayer structure. However, the mutual inductance is not limited to adjacent wires and layers and it exists among all parallel wires. The performance and reliability of the circuit is affected by multiple effects of parasitics. These parasitics result in crosstalk noise, propagation delay and power dissipation which affects the signal integrity and degrade the circuit performance.

The crosstalk is the coupling of energy from one wire to another via coupling parasitics and adversely affects the circuit operating at higher frequencies [8]. Crosstalk induces faults in the circuit which are glitch and delay faults. The crosstalk induced overshoot and undershoot generated at the circuit node can cause false switching and creates a logic error [9]. A crosstalk induced delay occurs when both the aggressor and victim lines are switching simultaneously. Mostly crosstalk induced delay causes chip failure more than crosstalk induced glitch. The propagation delay and crosstalk noise in high frequency chips are dependent on the value of parasitics per unit length of interconnect [10]. Because of severe effects of parasitics, the optimization of parasitics for their effects is an important area of study.

A great deal of research has been done on the analysis of crosstalk noise [11], [12], [13], [14], [15], [16], [17]. The minimization of crosstalk using different techniques *viz*. resizing drivers, shielding interconnects, rerouting signal, bus encoding and repeater insertion has been reported in [18], [19], [20]. Researchers have reported the optimization of interconnect models/circuit using different approaches [21], [22], [23], [24]. Apart from the literature available, research is needed in the area of optimization of coupling parasitics taking into account the severe effects of crosstalk noise and delay. In [25], the optimization of coupling capacitance for delay and peak noise using qualitative approach is reported.

This paper presents a qualitative approach to optimize both mutual inductance and coupling capacitance collectively for delay. This paper also addresses the optimization of driver width qualitatively for crosstalk noise/delay. The optimization of driver width is equally important because it has effects on crosstalk noise and delay. The interconnect designers sometimes increase driver width to reduce propagation delay which may lead to increase in crosstalk level. The SPICE simulations are run and various waveforms are obtained at far end of interconnect lines.

Following this introduction, the paper is organized such that Section 2 describes the simulation setup for coupled lines. The effects of coupling parasitics and driver width are discussed in section 3. The optimization of coupling parasitics and driver width for delay and peak noise for simultaneously switching inputs is carried out in section 4 and simulation results are discussed. Finally, section 5 draws necessary conclusions.

2 Simulation Setup

In this work, two distributed *RLC* lines coupled inductively and capacitively are used for simulation as shown in Fig.1. The distributed model is the most accurate approximation of the actual behavior than the traditional lumped *R*, *L*, *C* model [3]. The length of interconnect is taken as 4mm and each line of coupled interconnects is 2µm wide, 0.68µm thick and separated by 0.24 µm [11]. Twenty distributed lumps of Gamma type are taken for the interconnect length under consideration. The capacitance and inductance values are obtained from the expressions available in [26], [27]. At far end of interconnect lines, CMOS load is replaced by 30fF capacitor. The interconnect parasitics for one meter length are represented by transmission line matrices in Fig. 2.

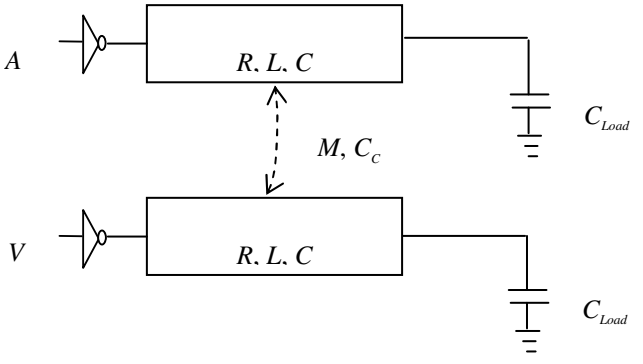

Fig. 1. Model of uniformly distributed coupled interconnect lines

$$R = \begin{bmatrix} 12{,}500 & 0 \\ 0 & 12{,}500 \end{bmatrix} \quad C = \begin{bmatrix} 190p & -64p \\ -64p & 190p \end{bmatrix} \quad L = \begin{bmatrix} 1.722\mu & 1.4\mu \\ 1.4\mu & 1.722\mu \end{bmatrix}$$

Fig. 2. Interconnect Parasitics

The simulations use an IBM 0.13µm technology with copper interconnect process (MOSIS) with a power supply voltage of 1.5V. The threshold voltages are roughly 10% of supply voltage. The transition time of the input ramp is taken as 25ps.

3 Effects of Coupling Parasitics and Driver Width

To capture the effects of coupling parasitics and driver width on peak noise and delay, SPICE simulations are run and various waveforms are generated at far end of lines by taking into consideration both the cases of simultaneous switching of inputs.

Case I: Both inputs are switching in same phase from high to low

Case II: Both inputs are switching in opposite phase *i.e.* aggressor input is switching from high to low and victim input is switching from low to high.

3.1 Effects of Coupling Parasitics

The effects of coupling capacitance and mutual inductance on peak noise and delay have been discussed and SPICE waveforms are shown in [17], [25]. From [17], [25], it is concluded that

(i) The propagation delay and peak overshoot noise increases with increase in the value of mutual inductance in same phase switching of inputs, however, the propagation delay and peak noise decreases with increasing mutual inductance in case of opposite phase switching of inputs. So, the peak noise and delay have same behavior against changes in mutual inductance in either case of inputs switching.

(ii) In same phase switching of inputs, the delay decreases while peak noise increases with increase in the value of coupling capacitance. In opposite phase switching of inputs, the delay increases while peak noise decreases with increasing coupling capacitance. So, in both the cases of inputs switching, the delay shows opposite behavior than peak noise against variation in coupling capacitance.

3.2 Effects of Driver Width

To observe the effects of driver width on peak noise and delay, the interconnect model under consideration is simulated for both the cases of inputs switching. The aggressor driver PMOS width is varied from 30-120 µm in steps of 10 µm, keeping the corresponding NMOS width half of the PMOS. The width of victim driver is kept fixed. The value of coupling capacitance and mutual inductance is taken as (480 fF, 5.6 nH). The simulation results obtained are shown in Fig. 3 and Fig. 4.

From the simulation results obtained in Fig. 3 and Fig. 4 for Case I of inputs switching, it is observed that the delay decreases while overshoot noise increases with increase in the value of driver width. Similar kind of results are obtained for Case II in which both inputs are switching in opposite phase.

4 Optimization: Observations and Discussions

The optimization of mutual inductance and coupling capacitance is carried out qualitatively for delay. Furthermore, the optimization of driver width is also presented. The basic idea of optimization process is from the fact that in some cases, the parasitic effects *i.e.* crosstalk noise and delay shows opposite behavior with change in the value of parasitics /other parameters.

4.1 Optimization of Coupling Parasitics

The optimization of coupling capacitance for delay and peak noise is reported in [25]. The qualitative optimization of mutual inductance is not feasible because of similar kind of behavior of peak noise and propagation delay. In this paper, the optimization of mutual inductance and coupling capacitance for specified range of values is carried out qualitatively for delay because it shows opposite behavior due to mutual inductance and coupling capacitance as discussed in the previous section. The simulation results are obtained for both the cases of inputs switching under consideration and are shown in Fig. 5 and Fig. 6.

4.1.1 Observations and Discussions

In Case I of inputs switching (Fig. 5), because of opposite tendency of delay due to mutual inductance and coupling capacitance, the curve for delay vs. M and the curve for delay vs. C_C crosses each other. Beyond this crossing point of the curves, if the values of M and C_C are increased, it is clear from the Fig. 5 that delay due to C_C decreases while it increases due to M. However, the behavior of delay is reversed if the values of M and C_C are decreased. Therefore, at crossing point of the curves in Fig. 5, the delay is optimized for some value of coupling capacitance and mutual inductance.

Similarly, in Fig. 6 in which the optimization is carried out qualitatively for Case II of inputs switching, it is observed that the coupling parasitics are optimized for delay at crossing point of the curves. From the results, it is clear that the optimal value of coupling parasitics is somewhere between 250-300fF and 3.8-4.2nH.

4.2 Optimization of Driver Width

The optimization of driver width for specified value of coupling parasitics is carried out qualitatively for both the cases of inputs switching and the results are shown in Fig. 7 and Fig. 8.

4.2.1 Observations and Discussions

From Fig. 7, because of opposite tendency of delay and peak overshoot noise due to change in driver width, the curve for delay and the curve for peak overshoot crosses each other. Beyond the crossing point of these curves, it is observed that delay increases while peak noise decreases with decrease in the value of driver width. These effects are reversed in behavior if driver width is increased. Therefore, the effects *i.e.* delay and overshoot noise for specified value of coupling parasitics are optimized at crossing point of the curves for some value of driver width. Similarly, the effects are optimized for some value of driver width for Case II of inputs switching as shown in Fig. 8. From the results, it is observed that the optimal value of driver width is somewhere between 40-50μm.

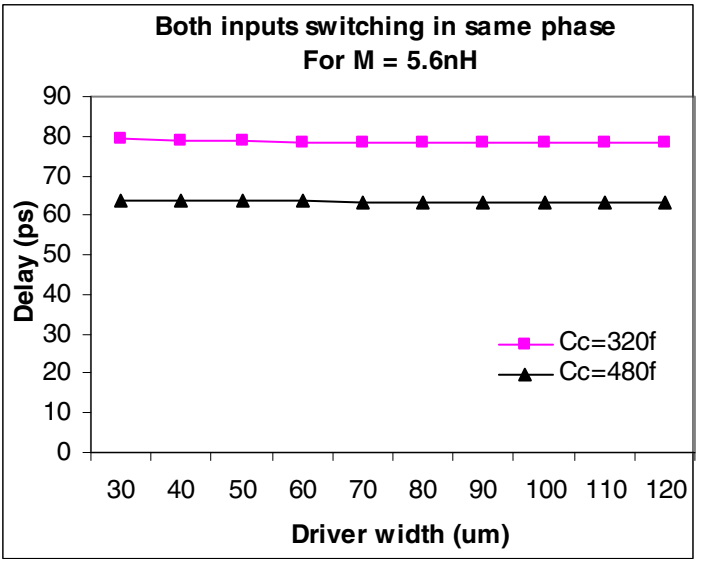

Fig. 3. Effect of driver width on propagation delay

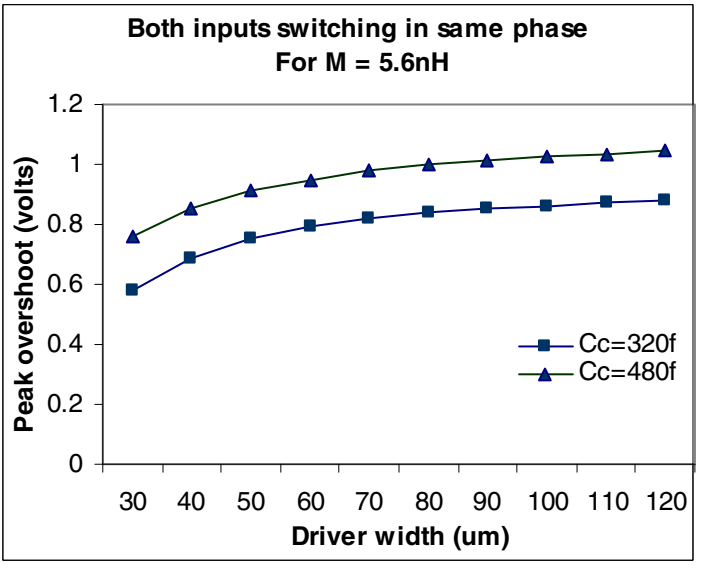

Fig. 4. Effect of driver width on peak overshoot noise

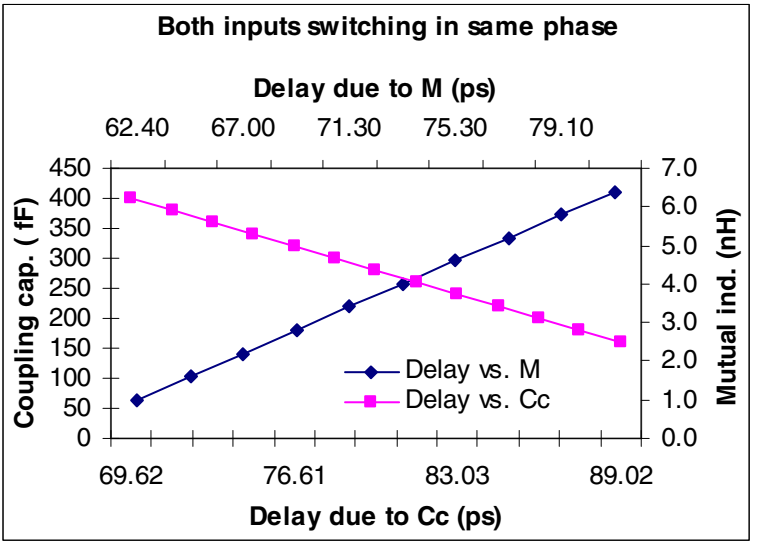

Fig. 5. Optimization of coupling parasitics for propagation delay in Case I

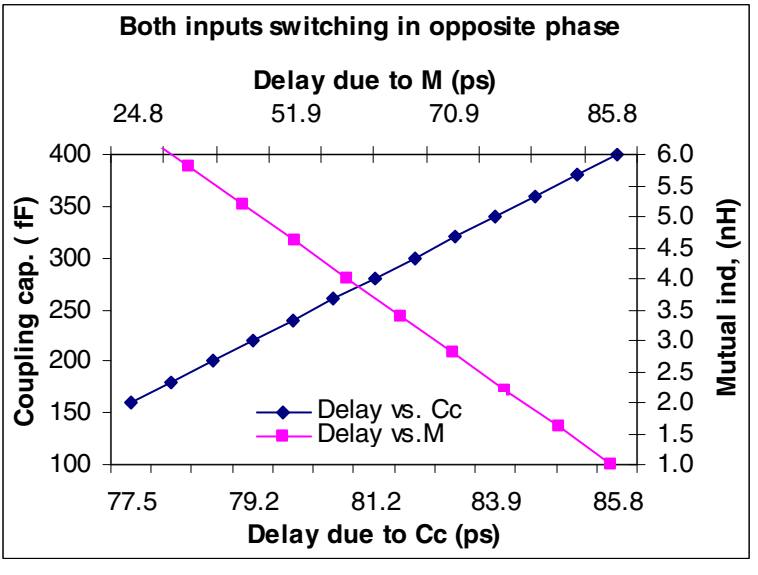

Fig. 6. Optimization of coupling parasitics for propagation delay in Case II

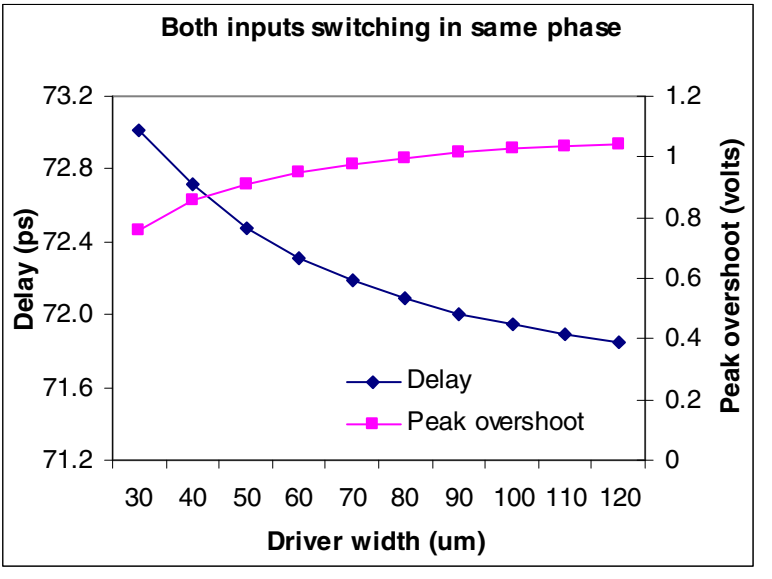

Fig. 7. Optimization of driver width for propagation delay and peak overshoot in Case I

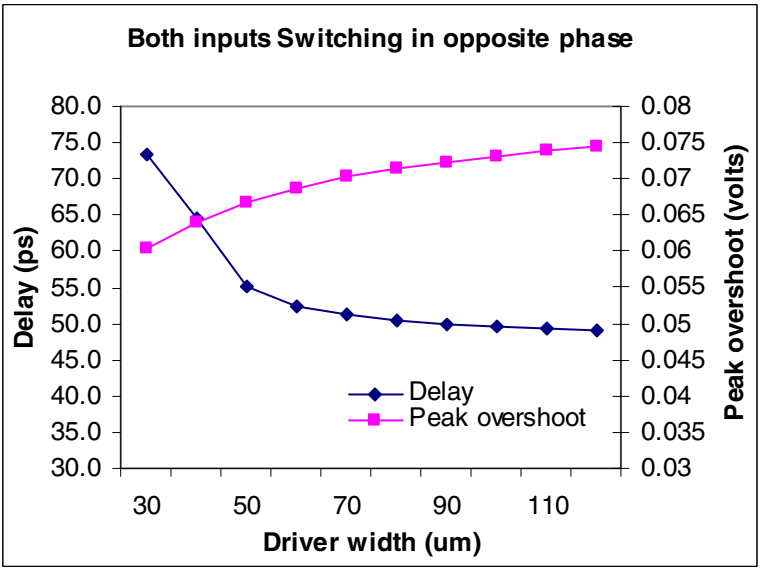

Fig. 8. Optimization of driver width for propagation delay and peak overshoot in Case II

5 Conclusion

A qualitative approach to optimize coupling parasitics and driver width for delay/peak overshoot noise is presented for simultaneously switching inputs. For both the cases of inputs switching, delay shows opposite behavior due to mutual inductance than coupling capacitance. Therefore, an optimum value of coupling parasitics (M and C_C) is observed that suggests the reduction of delay optimally. The optimal value is found to be somewhere between 250 to 300 fF and 3.8 to 4.2 nH. Similarly, on the basis of the effects of driver width observed on delay and peak noise, the optimization of driver width for these effects is carried qualitatively. The optimal value is found to be some where between 40-50 μm.

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