Realization of SDR in Partial Reconfigurable FPGA Using Different Types of Modulation Techniques

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Abstract. The increase in the consumer demand and the exponential growth for wireless systems, which enables consumer to communicate in any place by means of information, has in turn led to the emergence of many portable wireless communication products. The present research works primarily targets to integrate as much as signal processing applications in a single portable device. Since integration through software applications compromises system speed, integration through hardware will be the better compliment. Software Defined Radio (SDR) Technology yields to achieve this small form factor system while keeping power consumption under the limit. SDR enables soft changeable system functionality, such as receiver demodulation technique. The flexibility of changing the receiver functionality in runtime is usually attained by FPGA. However, using a complete FPGA for reconfiguration of a particular functionality is not an efficient method in terms of power consumption and switching time. We proposed a SDR architecture using a recent advancement in FPGAs, called Partial Reconfiguration (PR). PR helps to change certain portion of FPGA, while the rest keeps functioning. It also reduces the total hardware usage and hence the power. The different demodulation technique and other signal processing application from an external memory unit can be loaded into FPGA PR modules while the other parts of FPGA doing a constant data processing.

Keywords: Partial Reconfiguration in FPGA, Modulation Techniques, Wireless communication.

1 Introduction

SDR is a collection of Hardware and software in which all the radio functions can be implemented using software coding or firmware on a processing system. These software can be alterable according to the applications in communication system. The processing systems include Field Programmable Gate Arrays (FPGA), Digital Signal Processors (DSP), General Purpose Processors (GPP), Programmable System on Chip (SoC) or other Application Specific Programmable Processors. The use of SDR technologies allows new wireless features like Third Generation (3G) and Fourth Generation (4G) capabilities to be added to existing Generation for mobile applications and radio systems without requiring new hardware.

N. Meghanathan et al. (Eds.): CCSIT 2012, Part I, LNICST 84, pp. 83–89, 2012.

By using SDR Technique a family of Radio products used in communication to be developed in common platform architecture and lot of research work is going on in this area allowing new products will come quickly into market. Since the software to be reused across radio products, the development cost reduces dramatically. This type of wireless communication enables the user to communicate with whomever they need to communicate and in whatever manner according to their wish. For example video call is available in Third generation. Likewise any type of applications can be include using SDR in a single chip. The main advantage SDR engineers is to provide a single radio transceiver capable of playing the roles of cordless telephone, cell phone(GSM and CDMA), wireless fax, wireless e-mail system, pager, wireless videoconferencing unit, wireless Web browser, Global Positioning System unit, and other functions still in the realm of science fiction, operable from any location on the surface of the earth, and perhaps in space as well.

The General block diagram of SDR is shown in Figure 1. The radio frequency signal comes from antenna is down converted to baseband frequency range with the help of transceivers. The analog to digital converter will give the digital data to the processing module. The processing module will be a combination of FPGA and DSP in most cases. FPGA will be reconfigured by DSP according to the incoming signals modulation scheme or depends on the user's interest. Finally the original message signal will be given to a respected sink device.

The SDR is software radio in which all the physical layers are software defined. It effectively uses the area in FPGA.

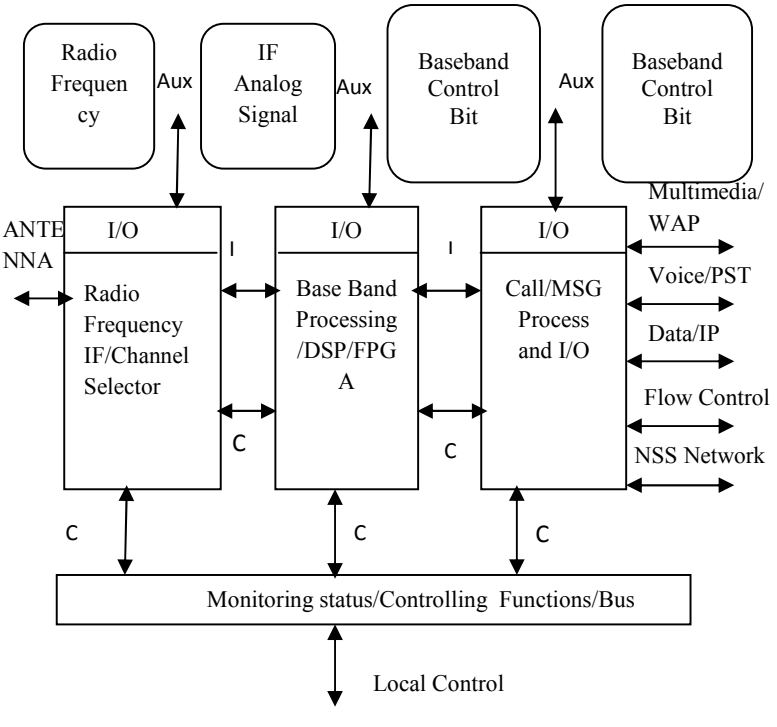

Fig. 1. Basic Diagram of SDR

2 General Implementation

The generalized implementation (block diagram) method of SDR system architecture is shown in figure 2. All software part is done in FPGA. This can be alter according to the applications.

The FPGA shown here is used for the soft reconfiguration and the DSP or any GPPs will do controlling of the FPGA and other data flow tasks. The combination of devices like DSP,FPGA, GPP is used in SDR, due to the advantage and disadvantage of each device.

DSP – good for software processing, branches but lack in parallelism.
FPGA– gives parallel architecture, high data rates but issues with software routine executions.
GPP– good for managing and controlling memories and peripherals but not optimized for algorithms development.

In most cases DSP is used because the combination of controlling ability and signal processing power. The different demodulation techniques configuration will be loaded into a memory unit initially. The choice will be given to user to select the required demodulation technique. Once the DSP receives the command to change the receiver demodulation, it reconfigures the FPGA by loading corresponding bit stream

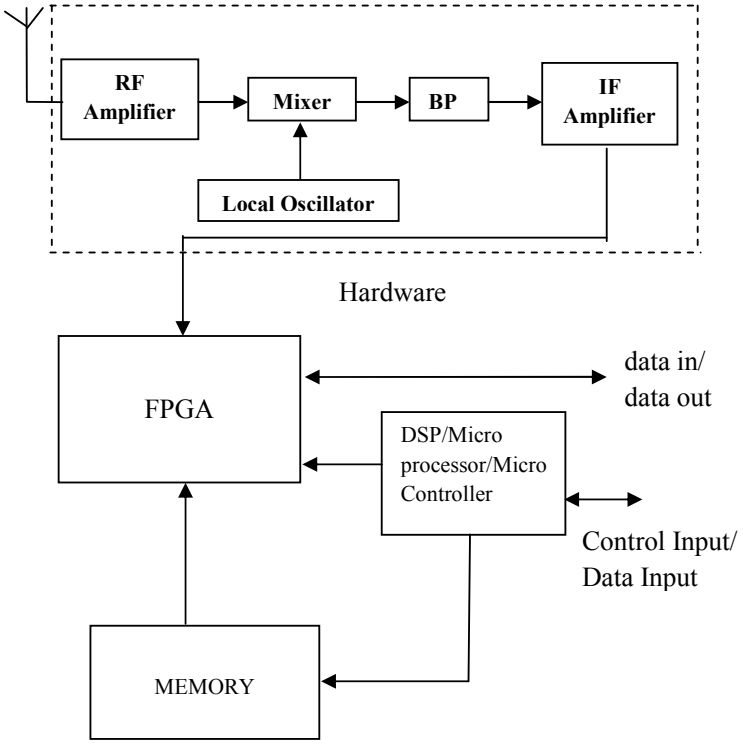

Fig. 2. General Implementation

from memory. Typical FPGA reconfiguration time will be in the order of 100s of milliseconds and this is huge delay when come into real time. Further this delay will increase if DSP running some other default communication task in parallel.

3 Proposed System Architecture

Due to the Rapid development in FPGAs, now we have all the following resources in single FPGA.

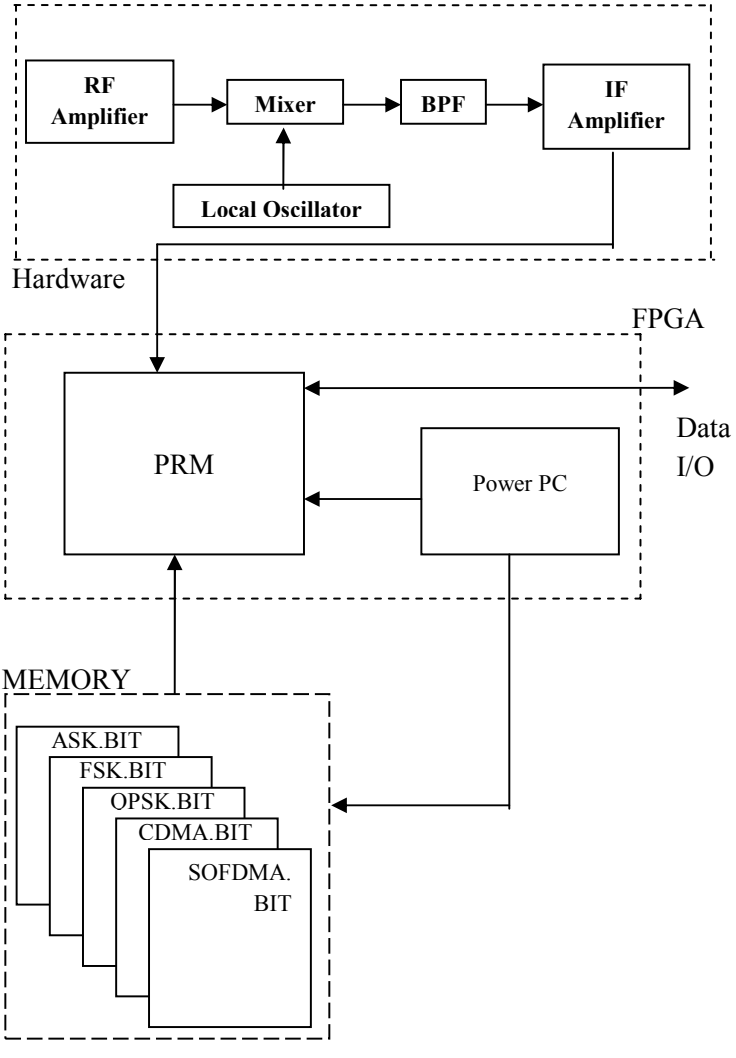

Fig. 3. Proposed system Architecture

Huge amount of Logic blocks: For more parallel logic designs.

DSP Slices: For signal processing algorithm implementation.

PowerPC: Embedded processor can be used as GPP. All these units can operate in parallel.

As shown in the block diagram, we have proposed a SDR architecture with only FPGA due to the availability of massive parallelism and Partial Reconfigurable ability. Since the newer FPGA provides PR modules, it is possible to change of the certain part of FPGA alone and hence we can avoid complete FPGA for reconfiguration. The embedded PowerPC and DSP slices can do a work of a GPP or DSP. Hence it is also not required to use dedicated ASIC for the controlling and signal processing purpose. The proposed architecture embeds everything into a single FPGA which in turn reduces the total resource utilization and hence the power and speed.

Our design mainly concentrates on runtime reconfiguration of demodulation techniques in Partial Reconfiguration blocks of an FPGA and keeping the rest of the baseband process unchanged. The modulation/demodulation techniques will be ASK, FSK, BPSK QPSK SOFDMA and CDMA.

4 Partial Reconfiguration

Xilinx introduced this method of reconfiguration to the market recently. As "Field Programmable Gate Array" name suggests, it gives user the flexibility to reconfigure the hardware on field instead of going through the complete ASIC design process for small modification or updation in the design. The new Partial Reconfiguration capability of recent FPGAs further enhances the flexibility by allowing partial configuration on an operating FPGA using partial bit files.

After a full bit file configures the FPGA, partial bit files can be downloaded to modify reconfigurable regions in the FPGA without compromising the integrity of the applications running on those parts of the device that are not being reconfigured.

As shown in Figure 4, the function implemented in Reconfigurable Block A is modified by downloading one of several partial bit files, A1.bit, A2.bit, A3.bit or

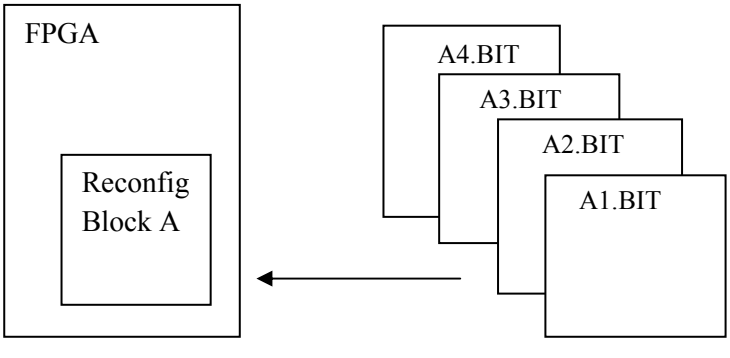

Fig. 4. Partial Reconfiguration in FPGA

A4.bit. The logic in the FPGA design is divided into two different categories, reconfigurable logic and static logic. The reconfigurable block A represents reconfigurable logic and the rest are static logic. The static logic remains functioning and is completely unaffected by the loading of a partial bit file. The reconfigurable logic is replaced by the contents of the partial bit file. There will be a Configuration controller which is part of the static module. This takes care of loading and unloading of dynamic modules. The command to this controller will be given from PowerPC with the reconfiguration data.

5 Conclusion

Realization of SDR in Partial Reconfigurable FPGA using different types of Modulation Techniques Developing using Xilinx FPGA. Due to the Realization is done by using the help of Partial Reconfiguration. The Speed and performance can be improved. The area also can be decreased. The New Xilinx, Vertex Series FPGA provides the provision of Partial Reconfiguration. The power Consumption can be reduced by applying power reduction Techniques in the blocks. In future, more types of modulation techniques can be done in same chip using Partial Reconfiguration with high performance.

This Receiver can be used in Mobile stations, Radio Stations etc. The use of Partial reconfiguration any function can alter at any time without affecting the current operation. The demodulation Techniques in the receiver side is stored in partial Reconfigurable blocks. The physical layers of SDR implemented in the FPGA.

6 Result

The Simulation is done by using Modelsim 6.4a. The Synthesis is done by using Xilinx ISE Software. The Simulation results are shown in the figure 5 and figure 6.

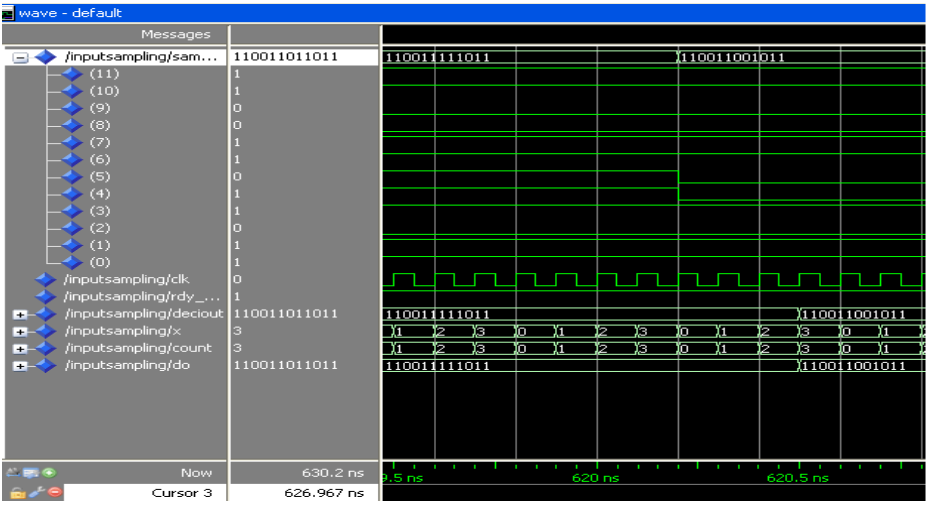

Fig. 5. Input Sampling in SDR

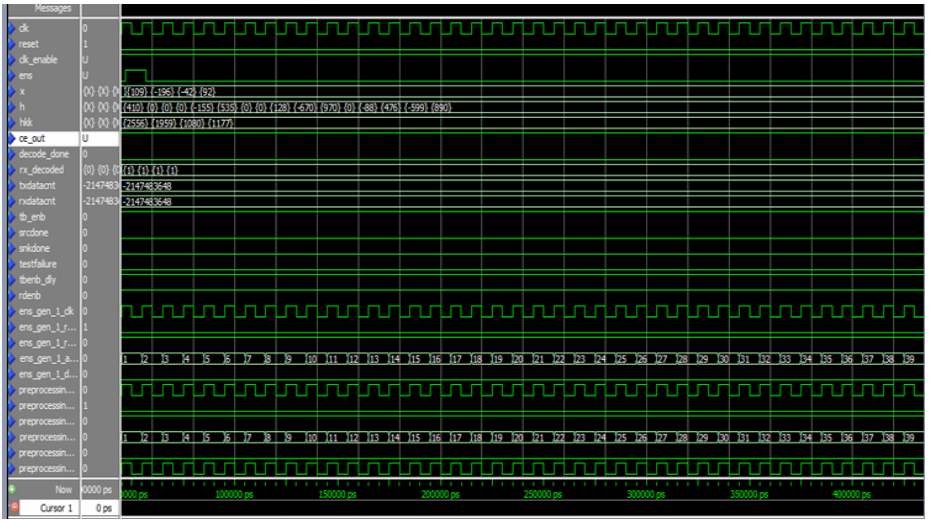

Fig. 6. Simulation Result

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