Low Power Spatial Modulation Scheme for Wide Band Multiple Input and Multiple Output Wireless Communication Systems

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Abstract. In this paper, we present design and FPGA implementation of a low power fractional bit encoded (FBE)–spatial modulation (SM) based transmitter for the multiple-input multiple output (MIMO) systems. This Modulation scheme includes the data dependency check before the spatial multiplexing. The proposed data dependency check allows efficient selection of antennas for parallel transmission of data. The Fractional bit encoding is modulus conversion scheme which convert the incoming bit stream to numbers in an arithmetic base, or modulus, that is not a power of 2 .When applied to SM, FBE results in a more versatile system design allowing transmitter to be equipped with an arbitrary number of antennas for a wider range of spectral efficiencies given restrictions on space and power consumption. The synthesis results of the implementation of transmitter on FPGA are included in the paper

Keywords: Low power, data dependency, Fractional Bit Encoding (FBE), Inter Channel Interference (ICI), Multiple input multiple output (MIMO) system, Spatial modulation (SM).

1 Introduction

Multiple Input Multiple Output (MIMO) transmission systems have been proposed to significantly increase the spectral efficiency of future wireless communications. A spectral efficiency of 20-40 bps/Hz can be achieved in the Vertical Bell Laboratory Layered Space Time (VBLAST) architecture when considering an indoor rich scattering propagation condition [1]. VBLAST is used in the multi user diversity scenario and various studies are reported in relation to it [2][3] . However, simultaneous transmission on the same frequency from multiple transmitting antennas causes high interchannel interference (ICI). This significantly increases system complexity as the number of transmitting antennas increases [2]. SM avoids ICI and the need of accurate time synchronization amongst antennas by making only one antenna active at any instant of time and employing the antenna index as additional source of information [4]. The use of transmit antenna number to convey information increases the spectral efficiency by a factor equals to $\log_2$ (the number of transmit antennas) [5]. In SM any group of information bits is mapped into two constellations; signal constellation based on the type of modulation and space constellation to encode

N. Meghanathan et al. (Eds.): CCSIT 2012, Part I, LNICST 84, pp. 631–639, 2012.

the transmit antenna number [4, 5]. At the receiver, maximum ratio combing is used. The detection process consists of two steps. The first one is the transmit antenna estimation while the second one is the transmit symbol estimation.

In SM, the number k of information bits that are encoded in the spatial domain is directly related to the number M of transmit antennas, in particular $M = 2^k$. This means that the number of transmit antennas must be a power of two. This paper implement a solution to this limitation in SM which increases the granularity of the data encoding process in the spatial domain by using fractional bit encoding; the method is called FBE–SM [8].These schemes do not consider the data dependency on the switching of antennas from the low power perspective. As shown in the present paper that by exploiting the data dependency with spatial multiplexing it is possible to achieve higher bit rate at low power consumption.

FPGA implementation of MIMO systems is reported in [9] while [10] reports FPGA based implementation of the VBLAST MIMO architecture. The aim of this paper is to implement and FPGA based FBE-SM transmitter which overcomes the limitation on the number of transmit antennas in SM and allow the transmitter to be equipped with an arbitrary number of antennas. In [11] a low power MIMO signal processor is designed however it was specific to the Ethernet application only. A layered based approach was suggested in [12]. The proposed approach divided the signal processing regions in the low power and high power however it do not discus about the data dependency on the power consumption. To the best of the authors knowledge this is the FPGA based implementation reported in literature.

The paper is organized as follows. In Section 2, the theory of fractional bit encoding is given. In Section 3, the FBE–SM scheme is introduced. In section 4 numerical results are shown to analyze the performance of FBE–SM, Section 5 gives the details of digital implementation of FBE-SM modulator and FPGA synthesis results and section 6 concludes the paper.

2 The Fractional Bit Encoding

Application of FBE to a pulse amplitude modulation (PAM) communication system is reported in [13]. It reports two ways of fractional bit encoding:

1)*Constellation switching-It* alternates between the transmission of D and D+1 bits per symbol to achieve the FBE. This approach suffers from the inherent bit shift that results from incorrectly decoded symbols making it prone to error propagation effects.

2)*Modulus conversion- This approach* minimize the error propagation effect that afflicts the performance of the constellation switching method [14]. In this paper the theory of modulus conversion is applied to SM.

Modulus conversion achieves fractional bit rates by converting the incoming bitstream to numbers in an arithmetic base, or modulus, that is not a power of 2. In particular, the modulus converter operates as follows: i) Extracting the blocks of PU bits from the incoming bitstream, where U is the desired fractional bit rate and $P$is a positive integer; ii) The extracted block is converted to P numbers of base R. The modulus is defined as the smallest integer number, R , such that $R \geq 2^k$.

Though the theory of modulus conversion can be used to achieve an arbitrary fractional bit rate, yet by choosing both R and P are positive integer numbers limits its application to only rational bit rates. However by using the inequality (1) it is possible to closely approximate U, with $\tilde{U}$ given as the ratio of two positive and relatively prime integers x and y.

$$0 \leq nU - \lfloor nU \rfloor \leq 1 \Rightarrow 0 \leq U - \lfloor nU \rfloor / n \leq 1/n \quad (1)$$

where $\lfloor . \rfloor$ denotes the floor function and n is an arbitrary and positive integer number. From (1), it follows that $PU \cong P\tilde{U} = P(\lfloor nU \rfloor / n)$, which, according to the theory of modulus conversion, must be a positive integer. It is worth mentioning that, in general, $P \neq n$. From (1) it can found that by selecting larger n is, the approximation error($U - \tilde{U}$) can be minimized. On the other hand larger P is, leads to greater error propagation within each block of bits[9].Accordingly, for any given U and provided that $P(\lfloor nU \rfloor / n)$ is a positive integer, $n$and Pshould be chosen as large and as small as possible, respectively.

3 The Fractional Bit-SM Scheme

As mentioned earlier FBE–SM scheme avoids fundamental constraints on the number of transmit antennas that can be used by classical SM systems. The fractional bit coding is done in the spatial domain, while the encoding process in the signal domain is left unchanged. Following guidelines can be used for designing a FBE-SM system [9]:

1)As per the system constraints(bit rate, cost, available space etc.) chose the desired number of transmit antennas, M,
2) Set the modulus R equal to M..
3) Compute the maximum spatial multiplexing gain offered by the system as $U = \log_2(M)$.
4) Choose the pair (P,n) $P(\lfloor nU \rfloor / n)$ is a positive integer and following the design guidelines described in Section II, *i.e.*:

   (a) Optimize $\tilde{U} = (\lfloor nU \rfloor / n)$, such that it is as close as possible to U This allows the system to approach the spatial multiplexing gain offered by the M transmit antennas. This is achieved, in general, for larger values of n.
   (b) Optimize P such that it is as small as possible: this reduces the decoding delay and, more importantly, minimizes error propagation in the decoded bitstream.

5) Map each of the P base–M encoded numbers in the transmission block to a transmit antenna index in the range[0,M-1].

Since at each time instant, only one transmit antenna of the set will be active. The other antennas will transmit zero power. Therefore, ICI at the receiver and the need to synchronize the transmit antennas are completely avoided. At the receiver, maximum receive ratio combining (MRRC) is used to estimate the transmit antenna number, after which the transmitted symbol is estimated. These two estimates are used by the

spatial demodulator to retrieve the block of information bits. The spatial constellation points (the base-M encoded numbers) are grouped into blocks of P points each, and each block is converted to the equivalent base–2 bitstream of $P(\lfloor nU \rfloor/n)$ bits each.

Let us consider a simple example with $M=6$ .Thus, we have U = 2.5850 By choosing, e.g. $(P,n)=(4,4)$, we get $\tilde{U}=2.50$, which closely approaches U and is greater than the spatial multiplexing gain offered by a system with $M = 4$. If, for instance, the block of $P\ \tilde{U}$ bits is equal to $(1010111011)_2$, then the modulus converter will return an $(P\ \tilde{U})_M$ block equal to $(3123)_6$ where $(x)_b$ denotes the base- b representation of x Then, the output of the modulus converter is mapped to a spatial constellation point. First, the antenna with index 3 transmits an energy signal, then the antenna with index 1 transmits the same signal, etc.

The receiver will estimate each received antenna index by using MRRC. After decoding the antenna indexes, ideally with no errors, it will recover the original data stream as: $(3123)_6 = (1010111011)_2$.

At Fig.1 and Fig 2 shows FBE-SM Transceiver architecture. We use the following notations: bold and capital letters denote matrices, bold and small letters denote vectors, $(.)^H$ and $(.)^T$ denote Hermitian and transpose of a vector or matrix, respectively. The FBE block encode numbers in the transmission block to a transmit antenna index in the range[0,M-1] while the signal domain encoding remain unchanged. . Then it maps the resultant symbols into a vector:$\mathbf{x=[x1\ x2\ ....x_{Nt}]}$, where it is assumed that $E_x[\mathbf{x^H x}]=1$; i.e unity channel gain. Since only one antenna is active, only one of x_j is nonzero in the vector $\mathbf{x}$. For the j^{th} active transmit antenna and the q^{th} symbol from M-ary constellation, the output of the SM mapping can be written as : $x_{jq}=[0\ 0\ 0\ldots x_q\ 0\ 0\ ..0]^T$[6]. This output of is fed to digital modulator to transmit the information to j^{th} subchannel. The signal is transmitted over a MIMO channel H=[h_1 h_2 …. h_{Nt}] and the corresponding Channel vector from the j^{th} transmit antenna to all receive antennas is $\mathbf{h_j}=[h_{j,1}\ h_{2,j}\ldots h_{Nr,j}]^T$ Each channel in the system can be modeled as Rayleigh flat fading Channel. The received signal $\mathbf{y = Hx + n}$, where n is Nr dimension additive white Gaussian (AWGN) noise $\mathbf{n= [n1,n2\ldots n_{Nr}]^T}$ The detection of information bits can be achieved by first estimate the antenna number then estimate the transmitted symbol according to the following rule [4, 6]:

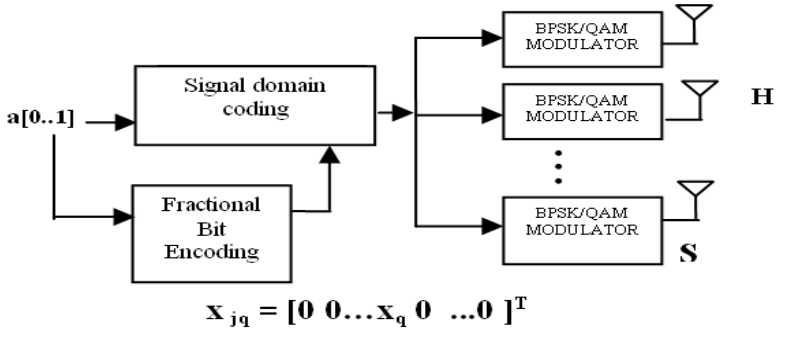

Fig. 1. FBE-SM Transmitter

$$\hat{j} = \arg_j \max | \mathbf{h}_j^{H} \mathbf{y} | \tag{2}$$

$$\hat{g} = \arg_q \max \mathrm{Re}\{(\mathbf{h}_{\hat{j}\,xq})^{H} \mathbf{y}\} \tag{3}$$

where $\hat{j}$ and $\hat{g}$ are the estimated Antenna number and transmitted symbol respectively.

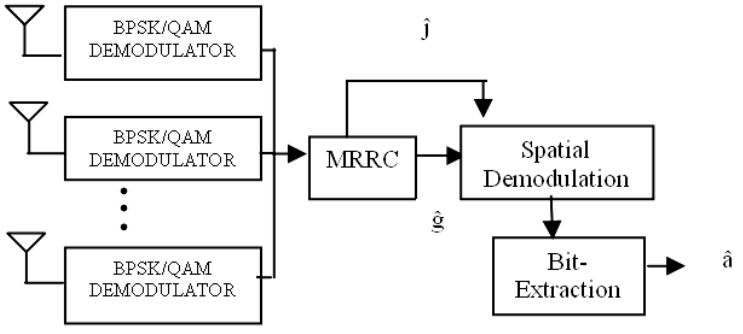

Fig. 2. FBE-SM Receiver

These two estimates are used by the spatial demodulator to retrieve the block of information bits. In the bit-extractor The spatial constellation points (the base-M encoded numbers) are grouped into blocks of P points each, and each block is converted to the equivalent base–2 bitstream of $P(\lfloor nU \rfloor / n)$ bits each.

4 Algorithm for the Data Dependent Antenna Selection

The proposed algorithm for data dependency check is given below. Input stream (I) is generated from LFSR. Total number of available antennas is known by its base value (B). Selection of antennas is also depends upon the input data stream as mentioned earlier . If the input is less than base value only one antenna is activated. For larger number base value several antennas will activate simultaneously. Thus checking the available free antenna can be utilized for next input stream of data. This can be done with parallel mode, so that the utilization of antennas will be more efficient than normal way of approach. This proposed algorithm is suitable for low power design approach of spatial modulation.

Algorithm DataDependencyCheck (I, B, A[], N, F[])

Input: LFSR input stream (I), Base value (B)
Output: Selection of antennas A[] with No. of Antennas N,
List of antennas F[] freely available for next Input Stream I_{NEXT}

Find the decimal equivalent (D) of input stream (I)
If D is less than or equal to B then

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                Assign D to A[0]
                Count the number of antennas N as 1
        Else
                Find Base B of D ( D_B )
                Store the digits of D_B in A[]
                Store the number of digits of D_B in N
        End if
        Find the free Antennas F[] from A[]
        The Antennas in F[] can be used in next Input Stream I_NEXT
End
```

5 Performance Analysis of Scheme

The following system setup is considered: i) Each transmit antenna, when activated, transmits a 4–QAM (quadrature amplitude modulation) signal. ii) The channel is assumed to be Rayleigh distributed with uncorrelated fading among the wireless links. It is static and flat-fading for the duration of a transmission block. iii) The noise at the receiver input is assumed to be white complex Gaussian, with zero-mean and mutually independent samples. iv) The receiver is equipped with 6 antennas and uses a MRRC detector to jointly detecting spatial and signal constellation points.

Two performance metrics will be investigated: 1) the symbol–error–ratio (SER), which is defined as the average probability of incorrectly detecting a constellation and signal point and 2) the bit–error–ratio (BER), which is defined as the average probability of incorrectly detecting a bit in the decoded bitstream In Figs. 3 and 4, we show the SER and BER of FBE–SM for various antennas at the transmitter, respectively. If $M = 2^j$, the system reduces to conventional SM. As expected Fig. 3 we notice that the SER gets monotonically worse for increasing values of M. However, this leads to an increase in the system bit rate When looking into Fig. 4 we observe that the BER does not get worse monotonically for increasing value of M. This is mainly due to the error propagation effect of the FBE process.

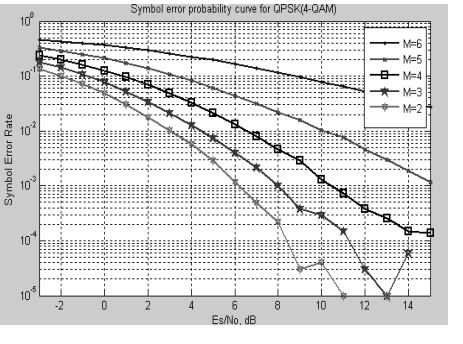

Fig. 3. SER of FBE–SM. for different values of transmit antennasM Setup: i) P= 4, and ii) n= 4

6 FPGA Implementation of FBE-SM

The implementation of FBE-SM transmitter is done on Cyclone-II EP2C35F672C6 family of FPGAs . The modulus conversion module which is integral part of the Fractional Bit encoding is replaced by the look up table. The approach to implement modulus converter as suggested by [11] require embedded multiplier and dividers which not only consume more silicon area but also consumes more power.

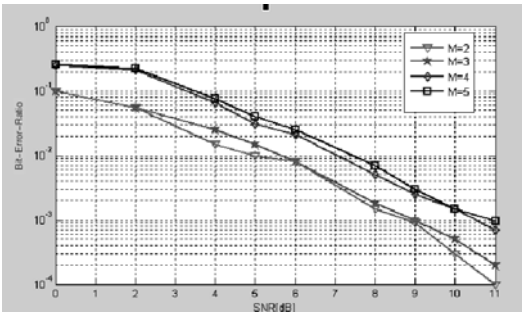

Fig. 4. BER of FBE–SM for different values of transmit antennas M Setup: i) P = 4, and ii) n= 4

Further more with the increase in the number of antennas, modulus converter size increases in turn it will require more number of multipliers and dividers and the highest speed to be achieved by the FBE-SM system will be limited by the size of modulus converter [8]. The look up table based approach is more area efficient and consumes less power. The reduction in power consumption is achieved by not using embedded multipliers and also with the help run time reconfiguration [13] design flow it is possible to update this look table for any arbitrary base at run time. A controller is designed to synchronize the operation of the FBE-SM transmitter module.The modulation scheme used is the 4-QAM (Quadrature amplitude

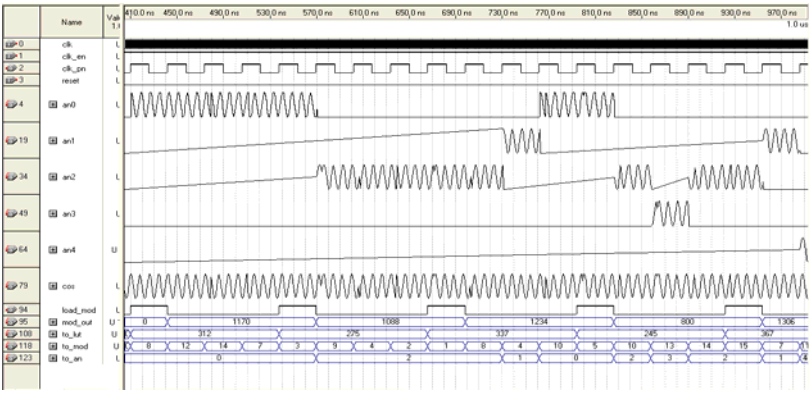

Fig. 5. Post Layout simulation Results for the Cyclone-II FPGA

Table 1. Resource Utilization Summary for Cyclone-II

SN.	Resource	Consumption
1	Logic Elements	546
2	Combinational Functions	497
3	Logic registers	280

modulation) or QPSK(Quadrature phase shift keying) .The modulator uses unrolled pipelined CORDIC structure which allows it to operate at the higher frequencies than the non pipelined CORDIC structure[14] . The intermediate operating frequency forthe transmitter is chosen to be 12.5 MHz. This can be up-converted to the desired frequency by using suitable RF front end. Table 1 shows the FPGA resources consumed by the FBE-SM transmitter. Fig. 5 shows the post layout simulation results of the FBE_SM implemented on the FPGA. The channel 5,6,7,8,9 are showing the output of FBE-SM transmitter for the antenna number one to five.

For the five antenna system the traditional FBE-SM transmitter consumes 6 mW dynamic power however the proposed solution consumes only 4mW dynamic power. Thus one third of dynamic power consumption can be reduced through this scheme.

7 Conclusion

In this paper we have implemented a more versatile low power SM scheme called FBE–SM on the FPGA. The method relies on the application of modulus conversion to achieve fractional bit rates, and allows any SM–MIMO wireless system to use an arbitrary number of antennas at the transmitter. By exploring the data dependency on antenna selection a higher data rate with low power consumption is achieved. MATLAB results for the SER and BER shows its viability for the design of compact mobile devices using SM. The proposed method offers the desired degrees of freedom for trading–off performance, low power consumption, highest achievable bit rates, and cost.

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