Carbon Nanotube Nanorelays with Pass-Transistor for FPGA Routing Devices

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Abstract. In this paper, a novel reconfigurable architecture, cFPGA (CMOS-Nanorelay FPGA) is developed by integrating carbon nanorelays and CMOS devices to function as FPGA components. cFPGA is a highly efficient architecture, providing 2X density and standby power improvement along with 30% dynamic power reduction as compared to the CMOS FPGA circuits. This performance improvement is achieved by using 2T1N structures as routing switches: Two CMOS transistors (2T): one for programming purpose and the other for signal transmission; one nanorelay (1N): the switching element. These 2T1N structures do not have nanorelays in the signal path, thereby eliminating the large quantum resistance in the path. This is a significant improvement over the conventional CMOS-nanorelay hybrid FPGA circuits. The proposed cFPGA is implemented using vertical carbon nanotubes which are relatively easier to fabricate as compared with horizontal nanotubes.

Keywords: FPGA, carbon nanotube, carbon nanorelay, nanoelectromechanical switch, CMOS-nano hybrid.

1 Introduction

Recent studies demonstrate that carbon nanotube (CNT) mechanical devices have potential in building low power FPGA circuits. This device can be used as a routing switch or a multiplexer logic gate in an FPGA. The simulation results show that this FPGA can have 30% less power consumption compared with the corresponding CMOS FPGA. The challenges in using this device in practice are: 1) Requires horizontal CNTs which are difficult to fabricate; 2) Always has two large quantum resistances in the signal path as the signal passes through two CNTs.

As commonly used CVD growth techniques grow vertical CNTs, vertical carbon nanorelays are proposed to be used as routing switches and can be used to connect CMOS logic blocks. However, this method has one CNT in the signal path. It is well known that a CNT has large quantum resistance. For SWCNT, the value is 6.5kΩ. The MWCNT has a slightly lesser value compared to SWCNT but is still quite large. Therefore, in order to use carbon nanorelay, new routing switches and the corresponding FPGA design need to be developed.

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In this paper, we propose a novel FPGA based on integration of carbon nanorelay and CMOS devices. By using a vertical nanorelay to control CMOS device, we can obtain a routing element with high-density, low-power and which does not have a CNT in the signal path. Based on this switch, we modify the routing circuit of FPGA, leading to an efficient cFPGA design. The delay and power of the FPGA depend strongly on the routing elements. This proposed device is expected to provide a significant performance improvement to FPGA chips.

The rest of the paper is organized as follows. Section II introduces the new nanorelay-CMOS routing switch. An electro-physical model is developed to analyze the device, which provides the guidelines for the fabrication of the device for cFPGA applications. Section III illustrates the cFPGA design to utilize the nano-relay-CMOS switches. Section IV discusses the performance evaluation results of the cFPGA. A comparative study is carried out to demonstrate the efficiency of the proposed cFPGA over the CMOS FPGA. Finally, we conclude the paper in Section V.

2 Novel Nanorelay-CMOS Routing Switch

The routing switch is generally a transistor which can be programmed "ON" or "OFF". When it is "ON", the signal in the signal path can be transmitted. When it is "OFF", the signal path is disconnected. This implements the basic routing function of the routing switch.

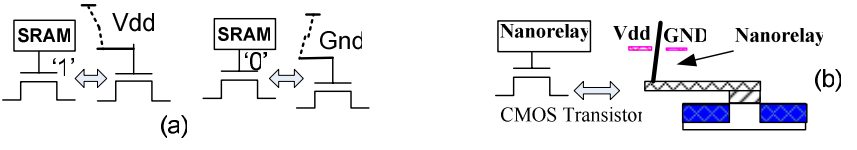

Fig. 1. (a) Conventional switching element and (b) Vertical nanorelay switching element

As shown in Fig. 1 (a), the currently used CMOS routing switch consists of a pass transistor controlled by a SRAM cell of 6 transistors to provide the routing function. The area of these 7 transistors is not trivial. Furthermore, in order for the 7-transistor (7T) SRAM cell to maintain the programmed bit, large standby power consumption P_{SRAM} is required.

Here, we propose a novel routing switch that consists of a nanorelay connecting to the gate terminal of a CMOS pass transistor. As shown in Fig. 1 (b), the CNT can be programmed to connect to the left contact to obtain a logic "1" i.e. the CMOS pass transistor is programmed "ON". Also, it can be connected to the right contact to obtain a "0" i.e. the CMOS pass transistor is programmed "OFF". The vertical CNT is located in a trench connected to a CMOS transistor. Therefore, the size of this proposed CNEMS-CMOS device is equivalent to only 1 transistor thereby providing a high-density routing switch.

Considering fabrication feasibility and the chirality control of the CNT, MWCNT is proposed to be used in the proposed device as it is difficult to control the chirality of SWCNT. However, in order to use this proposed nanorelay-CMOS device into

FPGA and get the low power operation, the programming voltage of the nanorelay needs to be around the CMOS device operating voltage i.e. around 1.2V. The length and diameter of the MWCNT and the size of the contact needs to be optimized for such specifications. Therefore, we carry out the following modeling and analysis to design the nanorelay for our applications.Papers not complying with the LNICST style will be reformatted. This can lead to an increase in the overall number of pages. We would therefore urge you not to squash your paper.

2.1 Modeling

The calculation of the threshold programming voltage of a nanorelay is based on the force balance between the carbon nanotube and the different electrodes. The total energy of the CNT is given by: $E_t = E_{vdw} + E_{elastic} + E_{electrostatic}$, where E_{vdw} is the energy sustained in Van der Waal's forces, E_{elastic} is the restoration energy in the CNT, $E_{\mathrm{electrostatic}}$ is the energy due the applied bias and E_{t} is the total energy.

The Van der Waals interaction energy between CNT and any electrode can be described by an empirical formula [1] $E_{vdw} = (-0.053 + 0.086d)a$, where d is the CNT diameter expressed in Å, a is the interaction length in Å.

The elastic energy can be calculated using the following $E_{elastic} = 1.6\delta^2 EI/L^3$ [2], where δ is the displacement of CNT's tip, E is the Young's Modulus, and I is the moment of inertia and it can be expressed from $I = \pi\left(d_1^{\,4} - d_2^{\,4}\right)/64$, where d_1 is the outer diameter and d_2 is the inner diameter of the CNT.

The electrostatic energy can be expressed as $E_{electrostatic} = CV^2/2$, where V is applied voltage, C is the capacitance between CNT and its adjacent electrode. The C can be approximated by assuming that the capacitor is formed between a cylindrical CNT and an infinite planar electrode plate. Therefore, $C = 2\pi\varepsilon_0 L/\ln(\delta/d)$, where ε_0 is the vacuum permittivity. In order to bend the CNT to connect with one electrode, a threshold voltage (V_{th}) is needed to be applied between the CNT and the electrode. The V_{th} can be calculated by setting $E_{electrostatic} = E_{elastic}$.

Therefore a general equation describing the relationship between different parameters can be expressed as $\left[\delta^2 E(d_1^{\,4} - d_2^{\,4})\ln(\delta/d_1)\right]/L^4 = 3.54\times10^8 V^2$.

For subsequent switching to connect to the other contact, the voltage can be calculated based on relationship of $E_{vdw} = E_{electrostatic} + E_{elastic}$. Combining all the equation, the general equation can be expressed as $1.376d_1 a - 0.085a = \left(7.85\times10^{-11}\delta^2 E/L^3\right)\left(d_1^{\,4} - d_2^{\,4}\right) + \left(0.0278LV^2/\ln(\delta/d_1)\right)$

The equations above can guide the design of the trench, the determination of the CNT size and the threshold or operating voltage. For instance, when d_1=3.5nm, d_2=2.8nm, E=1.3GPa, δ=10nm, equation (2) can be simplified as $L^2V = 5844.36$.

Based on simulation results using these equations,, we consider a nanorelay in this study with dimensional features d_1=3.5nm, d_2=2.8nm, E=1.3GPa, interaction distance δ=10nm, L=60 nm. The threshold voltage required to swath the CNT is 1.62V. The second switching voltage for an interaction length a=1.221nm is 1V.To ensure that

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3 cFPGA Design

cFPGA maintains the architecture of the baseline FPGA while utilizing nanorelay-CMOS devices to efficiently build several FPGA routing components.

As shown in Fig. 2, baseline FPGA consists of switch block (SB), connection block (CB), and logic block (LB). The routing resources include SBs, CBs, configuration memories, and interconnects, which account for around 70% of the total area, delay, and power of the FPGA (both local and global interconnects are considered) [2]. Thus, the improvement of these programmable routing elements by using the proposed nanorelay-CMOS switches will determine the FPGA performance. Specifically, the proposed cFPGA includes new CB and SB designs to utilize nanorelay-CMOS components. Note that the LB is still the traditional CMOS LB.

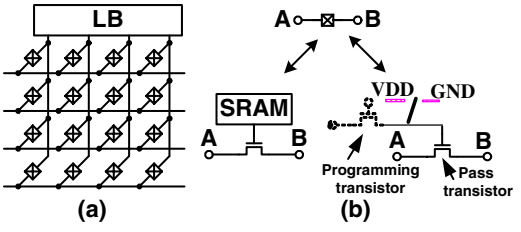

Fig. 2. (a) 4×4 CB structure (b) Replacement of a 7T switch with a 2T1N switch

3.1 Proposed CB Designs

The LBs connect to the routing channels through CBs. The existing 4×4 CMOS CB is shown in Fig. 2 [5]. By using the nanorelay-CMOS switch and one additional programming transistor to replace the 7T SRAM switch, we can obtain a high-density and low-power design (Fig. 2 (b)), namely, 2T1N.

3.2 Operation of 2T1N

The typical operation of the programming transistor is as follows. 1) The V_{dd} and GND terminals are set to 1.2V and 0V respectively. The threshold voltage, as calculated above, is 1.62V. 2) For a 2V programming pulse, the nanorelay considered in Section II connects to GND. 3) Next, with a -1V programming pulse, the CNT connects back to V_{dd}.

We also consider the use of the 2T1N switch to replace the 7T switch in the CB (see Fig. 2). For a 4×4 CB, 16 pass transistors and 16 programming nMOS are required. During operation, the 2T1N switch has the same delay as the 7T SRAM switch due to the use of pass transistor. The standby power saving while using 2T1N switches for the 4×4 CB is $16P_{SRAM}(5/6)=13.3P_{SRAM}$,as the power of the two junctions is equivalent to that of a CMOS transistor.

3.3 Proposed SB Designs

The CBs will connect to the SBs to establish the global routing. The function of a 1-bit SB is to connect one input terminal to one of the three output terminals. SB designs are based on either pass transistor or multiplexer. The pass transistor-based designs [6] are generally used in modern FPGAs and are considered here. The two typical 1-bit SB designs [7], namely SB-1 and SB-2, are shown in Fig. 3 (a) and 3 (b). SB-1 requires the 4 tristate buffers and SB-2 does not require the tristate buffers.

By using the proposed 2T1N switch to replace each 7T SRAM switch in Fig. 3 (a) and 3 (b), we can obtain nanorelay-based designs for SB-1 and SB-2 in Fig. 3 (c) and Fig. 3 (d) respectively. Each 1-bit SB has 4 identical branches and only one branch is illustrated here. The equivalent circuits of the branches for SB-1 and SB-2 are also included in the figure.

Table I summarizes the performance of these SB designs as well as the CB designs for the 4-bit operation. Therefore, four SB-1 or SB-2 blocks are considered to work with one 4×4 CB.

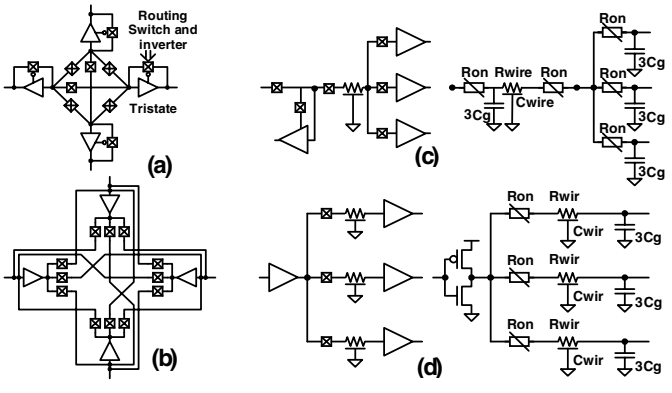

Fig. 3. (a) SB-1: CMOS design [7], (b) SB-2: CMOS design [7], (c) SB-1: RRAM design (4 branches are required; only one branch is shown) and its equivalent circuit, (d) SB-2: RRAM design (4 branches are required; only one branch is shown) and its equivalent circuit

Table 1. Performance Comparison of CB and SB Designs for 4-Bit Operations (1 pMOS is equivalent to 2 nMOS)

		CMOS SRAM designs	2T1N-based design
4x4 CB (Fig. 2)	Area (#nMOS)	324	8
	Standby Power	16 P_{SRAM}	-
4 SB-1's (Fig. 3 a,b)	Area (#nMOS)	520	240
	Standby Power	40 P_{SRAM}	-
4 SB-2's (Fig. 3 c,d)	Area (#nMOS)	528	192
	Standby Power	48 P_{SRAM}	-

In the baseline CMOS FPGA [1], the interconnects between two adjacent SBs are local interconnects, and additional HEX lines are used to connect two SBs to provide fast and direct connection. Our proposed SB designs can also have these interconnects, maintaining the interconnect structures of the baseline FPGA [1].

4 Performance Evaluation

In order to demonstrate the efficiency of the proposed cFPGA, we carry out a detailed performance evaluation and comparative study. We first estimate the performance of the complete cFPGA chips. Then, we simulate the FPGA benchmark circuits in cFPGA and compare the simulation results with the corresponding CMOS FPGA.

It is easy to see that the cFPGA can provide 2.5X higher density (logic) than the baseline 2D FPGA by utilizing RRAM circuits as FPGA components.

In terms of the critical path delay of the cFPGA block memory, the proposed design has the same delay value as the SRAM. The power consumption of cFPGA consists of the dynamic power and standby power. Both power consumptions are considerably large and are important to determine the FPGA performance. The dynamic power depends on the switching activities of the circuits implemented inside the FPGA, which can be estimated by simulating the benchmark circuits. For the CMOS FPGA, the LBs are assumed to account for 40% of the standby power and the routing resources are responsible for 60% of the power [1]. By using 2T1N routing switches, the 2D cFPGA can have more 2X improvement (logic) and 6X improvement (memory) over the CMOS FPGA in terms of the total standby power.

5 Conclusion

In this paper, we have introduced a new FPGA platform, cFPGA, to utilize RRAM circuits as memory and routing resources. cFPGA has the following superior properties. By using nanorelay to control the pass transistor, the proposed CMOS-nanorelay device does not have large quantum resistance in the signal path, leading to high performance operation. 1T1N-like CMOS-nanorelay devices are CMOS-compatible to establish FPGA CB and SB circuit and are naturally integrated with CMOS LB circuits to build cFPGA. The cFPGAs maintain the existing designs and CAD tools of CMOS FPGA.

Novel 2T1N routing switches can work as low leakage (static power) devices and significantly reduce the complexity of FPGA routing resources, enabling cFPGA to have 2X-3X density, 2X static power and 30% dynamic power improvement over the CMOS FPGA. Due to the aforementioned superior properties, cFPGA is expected to lead to innovation and technology breakthroughs in establishing reconfigurable platforms for the future nanotechnology era.

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