On Wires Holding a Handful of Electrons

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Abstract. When analyzing reliability, wires have in most cases been ignored, with gates (and devices) taking the lion's share. With scaling, this *"only computing fails"* approach is not going to be accurate enough as *communication (wires) will also start to err*. Trying to do justice to wires, this paper details a statistical failure analysis of wires following on the few papers which have made wires' reliability their concern. We will use a classical particle-like probabilistic approach to enhance on the accuracy of wires' length-dependent probabilities of failure due to the discreetness of charge. Covering some of the intrinsic noises, such an approach leads to "lower bound"-like wire reliability estimates, as ignoring other intrinsic noises, as well as extrinsic noises, variations, and defects. These results should have implications for multi-/many-cores and networks-on-chip, as well as forward-looking investigations on emerging nano-architectures.

Keywords: Nano-electronics, communication, interconnects (wires), noise (intrinsic), reliability.

1 Introduction

The fact that that electrical current is carried by quantized charges has been known for over a century, yet this discreteness has not affected us so far. Unfortunately, computers are currently heading towards several fundamental limitations. The most daunting ones comes from the fact that we are still relying on classical physics and mathematics—all of us have learnt in school—for the design of the hurly-burly rush of trillions of electrons through billions of wires and transistors. But, the chips at the heart of today's computers are running out of steam … in fact electrons!

Two issues become acute when transistors approach 10nm. One is that the formerly well-behaved electrons will start revealing their inherent quantum nature darting across the transistors on the dictates of probability, regardless of whether these are 'on' or 'off'. At those infinitesimal dimensions, where electrons will begin showing their true colors, computer makers will face hard choices: contain such quantum weirdness (with radically new types of devices), embrace the weirdness, or abandon the electrons (as the information carrier workhorse) and switch to something else. In fact, at below 10nm, any electronic (nano-)device and (nano-)wire will behave randomly due to both defects (*e.g.*, an electron might be trapped by a dangling bond, an unavoidable atomistic defect), and faults (*e.g.*, intrinsic noises). These will allow or

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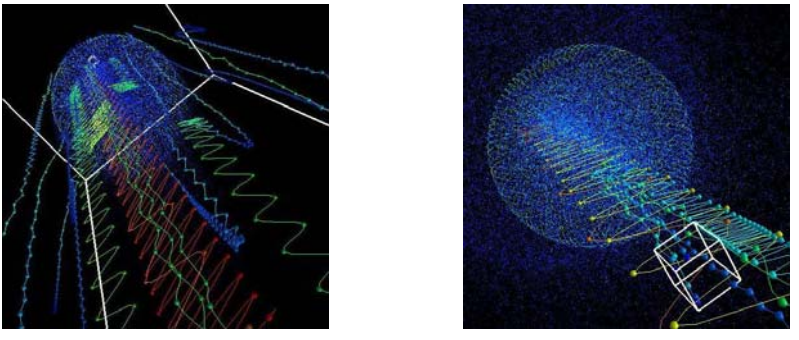
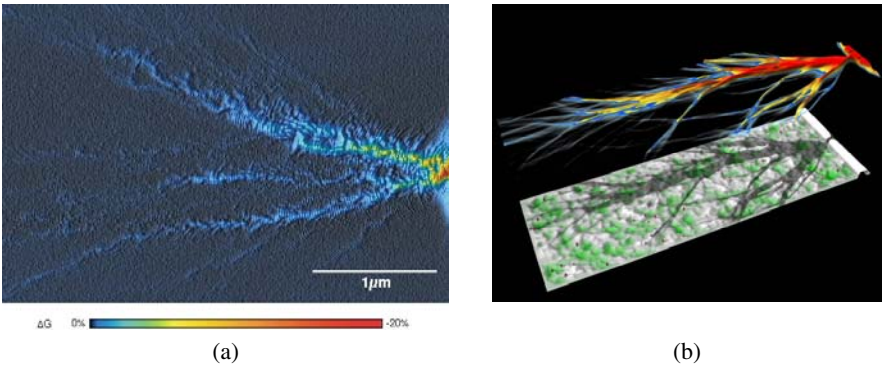
block (actually transmit, reflect, or scatter) electron movements, and the quantized current will turn 'on' and 'off' at random, as trapping/detrapping and also tunneling will occur stochastically. *This type of behavior is entirely contradicting the deterministic designs the semiconductor industry has been constantly relying upon, while it is routinely carried out by the many ion-channels forming our synapses* (at slightly less than 1nm, ion-channels are agitated by thermal noises opening and closing on the dictates of probability). To get a feeling of how electrons "flow," we present simulations/visualizations in Fig. 1, while Fig. 2 shows both measurements and simulations revealing quantum (wave-like) behavior.



(a) (b)

Fig. 1. Electron cloud visualization using AVS/Express show electron trajectories (as the simulation progresses), and track the movement of groups of particles (through the lifetime of the simulation). Trajectories were selected interactively with a box widget in the projection of the last simulation step, and were rendered as splines colored by the magnitude of their velocities. Courtesy of A. Adelmann, Visualization Group, Lawrence Berkeley National Lab (http://www-vis.lbl.gov/Vignettes/AAdelmann2004/phsp_trajectories/index_trajectories.html).



(a) (b)

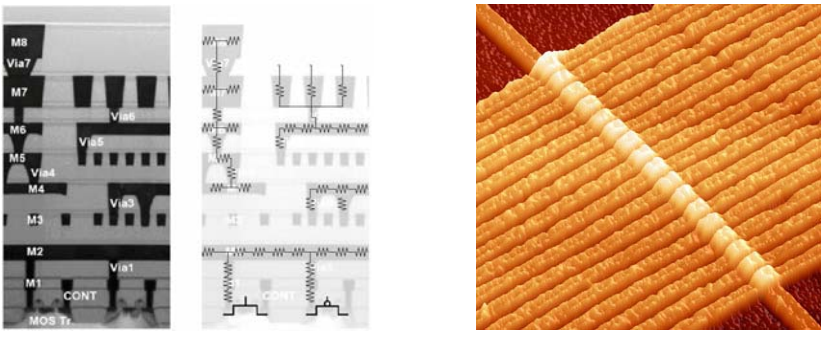
Fig. 2. Electron flow away from a quantum point of contact formed in a 2D electron gas inside a GaAs/AlGaAs heterostructure show that small angle scattering causes branches of electron flow to from at distances less than the mean free path: (a) measurements (using a scanned probe microscope) [1], [2]; (b) computer simulations showing both the potential which scatters and the calculated flow [3], [4]. From the image gallery of the Division of Condensed Matter Physics of the American Physical Society (http://dcmp.bc.edu/page.php?name=gallery).

The other issue is also subtle, namely that when the number of electrons decreases many of the statistics associated to (some of) their collective behaviors are starting to exhibit Poissonian distributions, departing (more and more) from the well-known (-behaved) Gaussian distribution.

In this paper we shall analyze electronic-based communications (interconnects/wires) only from a statistical point of view. A classical particle-like probabilistic approach will be detailed and used to estimate wires' probabilities of failures when holding only a few electrons (*i.e.*, at low electron densities). We shall start by revisiting wires while briefly mentioning previous results. Afterwards, we will detail our fresh results and conclude.

2 On Scaling the Wires

Scaling is already raising major power and reliability concerns [5], while for future nano-devices, the interconnection (communication) challenge is only going to get worse [6]–[8]. Besides the obvious performance-related problems—increased delays and rising power—associated with interconnect scaling, several other issues are very troublesome (resistivity degradation, material integration issues, high-aspect ratio, wire coverage, planarity control), leading to *a plethora of reliability-related concerns*. Equally important, some other problems are increasing with scaling: poor pattern definition, line-edge roughness, nano-scale corrosion, low-*k* dielectric cracks, post-chemical-mechanical polishing residues, to mention just a few. To get an understanding of the current state-of-the-art Fig. 3(a) shows a cross section of a multilevel wire stack, while Fig. 3(b) presents wires crossing (from [9]).



(a) (b)

Fig. 3. (a) Cross section of a multilevel wire stack (and its equivalent network). (b) Crossing of wires (courtesy of HP) [9].

It is almost two decades ago that Miller [10] clearly stated that semiconductor chips suffer from an impedance matching (or voltage-transforming) crisis which will only be aggravated by scaling: "*Small devices carry small currents and are therefore essentially high-impedance (and low-capacitance) devices, both for outputs and inputs, but electrical transmission is unavoidably low impedance (or high capacitance*

per unit length)"—a fact recently reemphasized by Yablonovitch [11]. In 2000, Sakurai [12] also drew the (now obvious) conclusion that the interconnects—rather than transistors—will be the major factor determining the *cost, delay, power, reliability and turn-around time* of the future semiconductor industry. Unfortunately, "*the miniaturization of interconnects, unlike transistors, does not enhance their performance*" [13]—as once interconnect scaling challenges are overcome, wires will still degrade delay and increase power consumption [5], [8].

With continued scaling, the copper (Cu) resistivity is increasing sharply due to interfacial and grain boundary scattering. Designers used to address this problem by increasing transistor channel width to provide larger drive currents (at the expense of reducing integration and increasing power). For example, in an older 0.1µm technology (using Al and SiO_2 dielectric), the transistor delay was 20ps, and the RC-delay of 1mm line was 1ps, while in a projected 32nm technology generation (using Cu and low-*k* dielectric) the transistor delay will be 1ps, and the RC delay of a 1mm line will be 250ps [14], [15]. In the next few years up to 80% microprocessor power will be consumed by interconnect [16], and these numbers will get worse as the technology is scaled further down (in 32nm, a 1mm wire will require 30× the energy of a transistor [5], [17]).

This communication challenge [13]–[15] has received less attention than power/heat [5], [8] and more recently reliability [18]–[22]. This is in spite of the fact that *communication is clearly bridging the power and reliability challenges as (high-speed) on-chip communications are getting more-and-more power hungry* (due to the large number of electrons needed to drive the wires [5], [8], [16]) *and less-and-less reliable* (or equivalently, more-and-more sensitive to noises, variations, and defects).

(a) (b)

Fig. 4. Scientific/artistic renditions: (a) A nanowire "[the image] grew out of a study of electron flow in a wire riddled with random imperfections; it shows electrons injected at one contact point … flowing out from there to all regions of the wire … the disturbance of the electron tracks by the imperfections [and] is shown in their somehow unruly paths [while] the quantum aspect of the electrons is shown in color" [28]. (b) A composite triple manifestation of chaos: two classical and one quantum; at the top of the image (the "sky") is a random wave, corresponding to the quantum manifestation of classical chaos; in the middle is a stroboscopic accumulation of the motion of a chaotic rotator [field]; in the foreground the motion of electrons in a nanowire is shown (the wire has some roughness in its shape attributable to the method by which it was produced), which causes electrons' trajectories to behave randomly over time. Both images courtesy of E.J. Heller (http://www.ericjhellergallery.com/).

Obviously, the discreetness of charge will unavoidably increase (some of) the intrinsic noises when approaching the mesoscopic regime (the transition from classical to quantum), and trying to negotiate beyond [7], [8], [23]–[27], and falls under the

focus of this paper. Before getting into the nitty-gritty details we present two more scientific/artistic renditions (Fig. 4) suggesting how the electrons might be moving on a nanowire (Fig. 4(a)), while a closer look reveals their chaotic behavior (Fig. 4(b)).

3 How Often Do Wires Fail?

There are many causes integrated circuits err, but one could immediately classify them into: intrinsic noises, extrinsic noises, variations, and defects. Here we shall consider only intrinsic noises, which make the results we will presented look like a "*lower bound*," as all the other causes of errors are only going to make things worse.

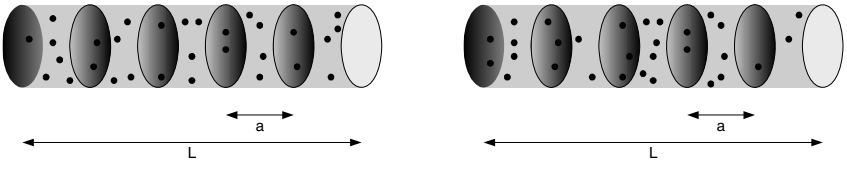
Let us suppose that a wire is connecting a transistor T_1 to another transistor T_2. The intrinsic noises could be translated by and large into variations of the distribution of the electrons along the wires. Thus, electrons would (in fact) be unevenly distributed along a wire, a possible example being suggested in Fig. 5. The communication between T_1 and T_2 fails (hence, *"the wire fails"*) when not enough electrons are available to drive the gate of T_2. One possible estimate of the wire's probability of failure (P_{wire}) in line with this abstraction was presented in [8]. To simplify the calculations of P_{wire} Cavin *et al.* [8] assumed that the wire is divided into a number of bins such that the capacitance of each bin equals the capacitance of the transistor's gate. Therefore, if the gate length is a and the wire length is L, the number of bins is:

$$b_0 = L/a. \tag{1}$$

(see also Fig. 5). The authors of [8] also assumed that to successfully drive T_2, the wire should have at least one electron in the last bin (connected to the gate of T_2). In case of a single electron on the wire, the probability that the electron would be found in the last bin is $1/b_0$, while the probability that no electron will be in the last bin is $1 - 1/b_0$ (supposing that the electrons move freely, while certain positions might be favored at small dimensions and low electron densities [29]). Finally, [8] assumed that the number of electrons on the wire n_{wire} has to be at least the number of electrons on the gate of transistor T_1 (n_{gate}). If $n_{wire} = n_{gate}$, the probability that the last bin has no electrons can be calculated as:

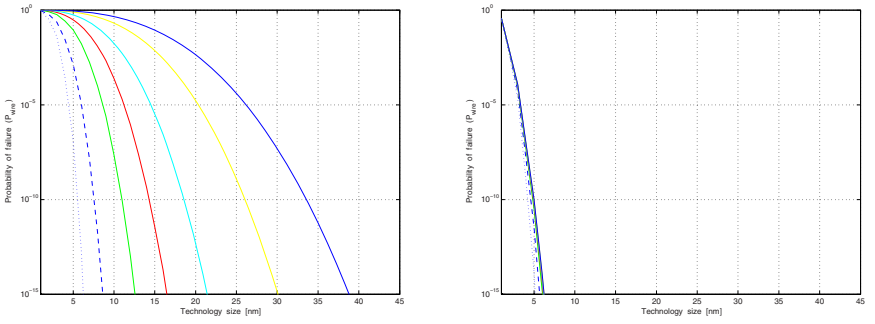
$$P_{wire} = (1-1/b_0)^{n_{wire}} = (1-1/b_0)^{n_{gate}}, \tag{2}$$

where $n_{gate} \approx 1.33a^{1.77}$ [30].



(a) (b)

Fig. 5. An L = 80nm wire driven by an a = 16nm transistor, *i.e.*, n_{gate} = 30 electrons, L/a = 80nm/16nm = 5 bins: (a) uniform 6, 6, 6, 6, 6; (b) non-uniform 6, 5, 9, 7, 3



(a) (b)

Fig. 6. Probability of failure of wires of length (from left to right): 10, 20, 50, 100, 200, 500, and 1000nm when driven by a device of size a: (a) when $n_{wire} = n_{gate}$ (eq. (2))[8]; (b) when $n_{wire} = b_0 n_{gate}$ (eq. (3))

Fig. 6(a) shows P_{wire} estimated using eq. (2). It is clear that, for the same feature size a, *longer wires have higher probability of failure than shorter ones*. For these calculations we have not limited the length L, while in fact L should be at least $3a$, as aptly pointed in [8]. This is why Fig. 6(a) should in fact show P_{wire} for the 10nm wire only up to 3.3nm feature size; for the 20nm wire only up to 6.6nm feature size; for the 50nm wire only up to 16.6nm feature size; etc.

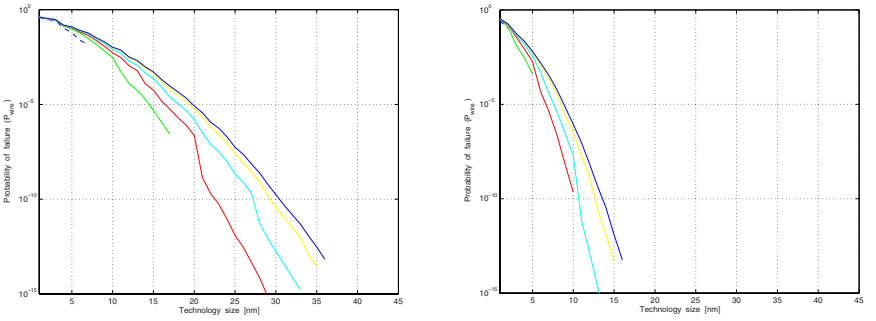
4 More Accurate Estimates

The previous result (eq. (2)) assumed $n_{wire} = n_{gate}$. However, when T_1 is 'on', it connects the wire to either V_{DD} or *GND* (assuming a standard CMOS gate). It follows that either V_{DD} will charge the wire, or the wire will be discharged to *GND*. That is why $n_{wire}/n_{gate} \approx C_{wire}/C_{gate}$, hence $n_{wire} = (C_{wire}/C_{gate}) \times n_{gate} = (L/a) \times n_{gate} = b_0 n_{gate}$, and:

$$P_{wire} = (1-1/b_0)^{b_0 n_{gate}}. \tag{3}$$

Fig. 6(b) presents the simulation results when using eq. (3) to calculate P_{wire}. It shows that, having more electrons on the wire ($b_0 n_{gate}$ instead of just n_{gate}) which is driving the next transistor T_2 reduces P_{wire} drastically (at the expense of increasing power).

Still, both eqs. (2) and (3) are based on the assumption that only a single electron is required to drive the gate of the next transistor T_2. This assumption represents the lowest possible number and cannot be valid in general (except for single electron technologies). Let us now suppose that in order to drive transistor T_2, at least γ electrons should be available on the transistor's gate (γ can be linked to the threshold voltage V_{th} of T_2). This implies that a wire fails if the number of electrons in the last bin (the bin connected to the gate of transistor T_2) is less than γ. In this case, P_{wire} can be calculated (based on exact counting arguments) as the probability that the number of electrons in the last bin is $\geq \gamma$:



(a) (b)

Fig. 7. Probability of failure of wires of length (from left to right): 10, 20, 50, 100, 200, 500, and 1000nm when using eq. (6) with $b_2 = 5b_0/12$, $\gamma = (2/3)n_{gate}$, and $\nu = 0.1$, *i.e.*, 10% noise (hence $n_{wire} = (1-\nu)b_2 n_{gate}$): (a) driven by a device of size a; (b) driven by a device of size $4a$

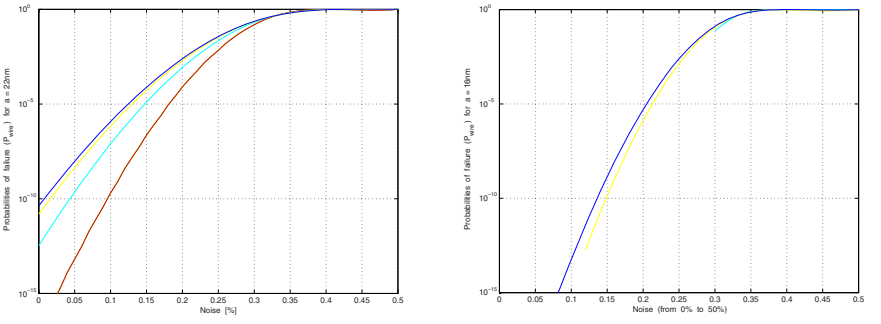
$$P_{wire} = \frac{\sum_{k=0}^{\gamma-1}\binom{n}{k}\times(b-1)^{n-k}}{b^n} = \frac{\sum_{k=0}^{\gamma-1}\binom{b_0 n_{gate}}{k}\times(b_0-1)^{b_0 n_{gate}-k}}{b_0^{\,b_0 n_{gate}}} = (1-1/b_0)^{b_0 n_{gate}}\times\sum_{k=0}^{\gamma-1}\binom{b_0 n_{gate}}{k}\times\frac{1}{(b_0-1)^k}. \quad (4)$$

Calculating eq. (4) exactly is non-trivial as it involves factorials of large numbers. One option is to use Stirling's approximation $n! \approx \mathrm{sqrt}(2\pi)\cdot n^{n+1/2}\cdot e^{-n}$. For achieving the highest possible precision we have used alternating multiplications and divisions:

$$P_{wire} = \frac{\sum_{k=0}^{\gamma-1}\binom{n}{k}\times(b-1)^{n-k}}{b^n} = \frac{(b-1)^n}{b^n}\sum_{k=0}^{\gamma-1}\frac{n!}{k!(n-k)!}\frac{1}{(b-1)^k} = \left(1-\frac{1}{b}\right)^n\left[1+\sum_{k=1}^{\gamma-1}\frac{n-k+1}{b-1}\cdot\frac{n-k+2}{2(b-1)}\cdots\frac{n}{k(b-1)}\right] \quad (5)$$

where n is n_{wire} (equal to $b_0 n_{gate}$) and b is the number of bins (b_0 in eqs. (2), (3), (4)).

For even more realistic approximations, one should also consider the different dielectric materials used: high-k for the gate [31], [32] and low-k for the wires [33] (see also [5]). These affect eq. (1) by changing the number of bins to $b_1 = (L\times\varepsilon_{\text{low-}k})/(a\times\varepsilon_{\text{high-}k}) = b_0\times(\varepsilon_{\text{low-}k}/\varepsilon_{\text{high-}k})$, which for an advance technology would give $b_1 = (2L)/(24a) = b_0/12$. Additionally, the fringe capacitance [34], [35] should also be included. For a quick estimate, we have used the aspect ratio (AR) of modern and future wires: 1.6–2.0 (see Fig. 3(a) and [5]), hence the multiplicative factor for C_{wire} is about $\chi = 1+2\mathrm{AR} = 5$. These adjusting factors lead to $b_2 = \chi b_1 = 5b_0/12$.



(a) (b)

Fig. 8. Probability of failure of wires of length (from top to bottom) 1000, 500, 200, and 100 nm versus the percentage of noise v (between 0% and 50%): (a) 22nm technology and device of minimum size a; (b) 16nm technology and device of size $4a$ (*i.e.*, 65nm)

Additionally, we could model the aggregated intrinsic noises (thermal, shot, 1/*f*, partition, quantum) by and large, as a percentage $0 \leq v \leq 1$, which will modify the number of electrons on the wire from n_{wire} to $(1-v)n_{wire}$. Incorporating all these corrections factors into eq. (4) we obtain:

$$P_{wire} = (1-1/b_2)^{(1-v)b_2 n_{gate}} \times \sum_{k=0}^{\gamma-1} \binom{(1-v)b_2 n_{gate}}{k} \times \frac{1}{(b_2-1)^k} . \quad (6)$$

Fig. 7(a) shows P_{wire} when using eq. (6) for $v = 0.1$ (*i.e.*, 10% noise), $\gamma = (2/3)n_{gate}$, and $b_2 = 5b_0/12$. Increasing the size of the transistors from a to $4a$ is the simplest solution and works well (see Fig. 7(b)).

Concerning noise, variations of 56fA on 1pA were measured in [24], *i.e.*, v = 5.6%; $v = 10\%$ was suggested in [36], [37]; simulations in [38] have shown variations of ±13 electrons out of 84 electrons, *i.e.*, $v = 15\%$. That is why, Fig. 8 details P_{wire} for different wire lengths when v is varied from 0% up to 50%. Obviously, P_{wire} goes to 1 when v goes to 50%, but increasing the size to $4a$ is clearly shown to be a very good solution—unfortunately, one for which the price is higher power consumption.

5 Conclusions

This paper has presented estimates of the probability of failure of wires due to the discreetness of charge. While previous work [8] could be considered as an overestimate of P_{wire} (Fig. 6(a)), this paper has first introduced an underestimate (Fig. 6(b)), followed by more accurate/realistic estimates based on: (*i*) exact (exhaustive) counting arguments; (*ii*) closer evaluations of n_{wire}, including the influence of high-k and low-k materials and of the fringe capacitance; and (*iii*) aggregating intrinsic noises as variations of n_{wire}.

The probabilistic results presented here can still be refined by correlating each particular distribution (of the electrons on the wire) with their associated energies

(the lowest energy levels being more probable). Alternatively, simulations like those presented in [39] could also be used to enhance on the results reported here. Finally, the results pertaining to wires should be integrated with statistics of V_{th} (which are linked to γ) [40], [41], for example by using EDA tools based on Bayesian Networks [42]. Basically, estimates of P_{device} (like those presented in [43]) and P_{GATE} (like those presented in [36]–[38], [44]) should be combined with P_{wire} (like the ones presented in this paper), and integrated with technological related results (like the ones reported in [45] for CNT), while power/energy estimates (based on n_{gate}, n_{wire}, and the RC-delay) could also be determined.

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