On the Reliability of Interconnected CMOS Gates Considering MOSFET Threshold-Voltage Variations

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Abstract. This paper discusses the effects of MOSFET threshold voltage variations on the reliability of nanometer-scale CMOS logic gates. The reliability is quantified in terms of the probability-of-failure of individual CMOS gates, which is obtained from extensive Monte Carlo simulations of these gates. The study considers different nano-scale CMOS technology generations and compares the effect of threshold voltage variations on the reliability at the gate level. The results presented here show a clear dependency pattern of reliability on the gate's input combinations (vectors). The results also show that both the NAND and Majority logic gates can tolerate up to 40% of threshold voltage variations in a 90nm technology, while only up to 20% at the 22nm technology node.

Keywords: Reliability, threshold voltage, CMOS, gates.

1 Introduction

The continuous miniaturization of transistors is facing many challenges, including the reliability of these devices. A large number of articles have reported advances in analytical models of reliability. On the design side, most studies considered reliability at the circuit and system levels, with fewer ones delving into the gate and device levels. It is clear that studies at the gate level are needed to quantitatively relate probability-of-failure to actual variations at the device level. In the nanometer regime, process variations are expected to have significant effects on the performance of transistors. These variations will change key transistor parameters, hence affect its characteristics. An essential transistor parameter is its threshold voltage. This study investigates the reliability of CMOS gates when the transistors are subject to threshold voltage variations. The study aims to quantify the effect of threshold voltage variations, on the reliability of nanometer-scale CMOS gates in different technologies. The reliability is expressed in terms of the probability of failure of individual gates. The latter is obtained from extensive Monte Carlo simulations of CMOS gates. The study considered the CMOS NAND and Majority (MAJ) gates.

This paper is organized as follows. Section 2 provides a review on related reliability studies. The modeling and simulation procedure is described in Section 3. Section 4 presents the results of this reliability investigation, followed by concluding remarks in Section 5.

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2 Reliability

As silicon CMOS technology is scaled into the nanometer regime, the reliability became one of the major concerns in designing practical nano-systems. The shrinking devices and scaled-down voltages make the devices susceptible to fabrication defects and transient failures. Progress in research work on the reliability of nanoelectronic circuits involves two aspects: *reliability analyses* and *design improvements*. Reliability analyses refers to techniques for estimating circuit reliability, and/or finding accurate error bounds of individual devices/gates for reliable operation of the overall circuit. Reliability design improvements, on the other hand, rely on various schemes and architectures (based on space, time, or information redundancy) for increasing reliability.

A large number of articles have been published on reliability analyses / improvements. However, most of these articles investigate the reliability at the gate / circuit level assuming a fixed value for the probability-of-failure of individual gates and devices [1]–[3]. In [1] a new multiplexing-based redundant design scheme was proposed. The new scheme is based on the use of MAJ gates. The article analyzes the performance of the multiplexing scheme for very small redundancies, using exact combinatorial arguments. In [2], the authors present a new noise-tolerant computer architecture that can enable the construction of reliable nano-systems comprised of noisy gates. The fundamental principles of this technique are parallel processing by redundant logic devices/gates/circuits, parallelism in the interconnects between components, and parallel restitution of intermittent signals. In [3] the reliability of different full adders was investigated. The probability-transfer- matrix method was used to evaluate the reliability of each full adder for different values of the gate's probability of failure.

At the gate and device levels, thorough investigations were performed for Single-Electron Technology (SET) in [4]. This study focused on the behavior of two multiplexing schemes in combination with gates subject to geometric variations affecting their elementary devices (capacitors). The two schemes under investigation were MAJ- and NAND-multiplexing. First, the elementary gates were compared in terms of their intrinsic probability-of-failure with respect to variations. Secondly, the two multiplexing schemes were weighted against the reliability enhancements they were able to bring into the system.

The effect of threshold voltage variations on the reliability has been studied at different levels. In [5] the impact of variations on power was thoroughly investigated. The article shows the strong effect of threshold voltage variations on power consumption. This is due to the exponential relationship between leakage power and threshold voltage. Very recent studies showed the effect of atomic level variations on the threshold voltage [6]. This article described simulation techniques for studying the effect of discrete random dopants on the threshold voltage fluctuations. It should be mentioned that the relationship between reliability and process variations was also studies at the system level. In [7], Greskamp *et. al.* studied the impact of threshold voltage variation on aging-related hard failure rates at the processor level and presented quantitative analysis of these effects.

3 Simulation of CMOS Logic Gates

The logic gates considered in this study are the well-known NAND-2 gate and the MAJ-3 gate. The latter was chosen because it provides an essential function for many reliability schemes since it is able to vote on several (redundant) values and produce a single output. The NAND-2 was implemented as a static CMOS gate (Fig. 1 (a)), but the MAJ-3 gate was not a clear cut case. Two possible implementations are the mirrored MAJ-3 [8] (Fig. 1 (b)) and the output-wired-inverters MAJ-3 [9] (Fig. 1 (c)). In [10] it was shown that the mirrored MAJ-3 gives a higher yield than the output-wired-inverters one, when they are operated in the subthreshold region. Since the focus of this study is on normal operation (above threshold), both implementations were simulated with a 50% range for threshold variations. The results show that the probability-of-failure depends on the input vectors (Fig. 2). The two implementations are comparable when the input vectors are in consensus (000 and 111). However, the mirrored MAJ-3 is more reliable for the other six input combinations. On average, the mirrored MAJ-3 is more reliable than the output-wired-inverters MAJ-3, therefore only the mirrored MAJ-3 was further used in this study.

The CMOS logic gates under investigation were simulated with TSpice [11], using the Predictive Technology Models (PTM) for nano-scale transistors [12]. Two technologies were considered: 90nm and 22nm. For each technology, the power supply value was chosen according to the recommendations of the International Technology Roadmap for Semiconductors [13]. The reduction of power supply voltage is driven by the need to reduce power dissipation and increase the reliability of gate dielectrics.

The effect of threshold voltage variations was quantified using an in depth Monte Carlo analysis. This generates random variations of the threshold voltage by drawing them probabilistically from a Gaussian distribution. For each value thus chosen, all analyses requested by the input file are performed, and the results recorded. This type of analysis was performed for different ranges of threshold variations. The Monte Carlo analysis was performed 100,000 times for each of the two gates and each range of variations (5% to 30% in steps of 5%), i.e., 2,000,000 runs. MATLAB modules were developed to automatically scan and analyze the collected data and calculate the probability of failure. The collected data includes the output of the logic gate. For data analysis, the noise margins were set at 25% of V_{DD}. Thus, an acceptable logic 1 is defined as at least 75% of the power supply (V_{DD}), and an acceptable logic 0 is defined as at most 25% of V_{DD}. The MATLAB module reads the output file and checks the output voltages against these acceptable values, and counts all the errors at the output of each gate. The number of errors is afterwards used to calculate the probability of failure of that particular gate.

4 Reliability of NAND and MAJ

The probability of failure of the NAND-2 and the mirrored MAJ-3 gates were obtained for different threshold voltage variations, different input combinations, and different technologies. The probability of failure of each gate at a particular technology was then estimated by averaging the values for all the input combinations. Fig. 3

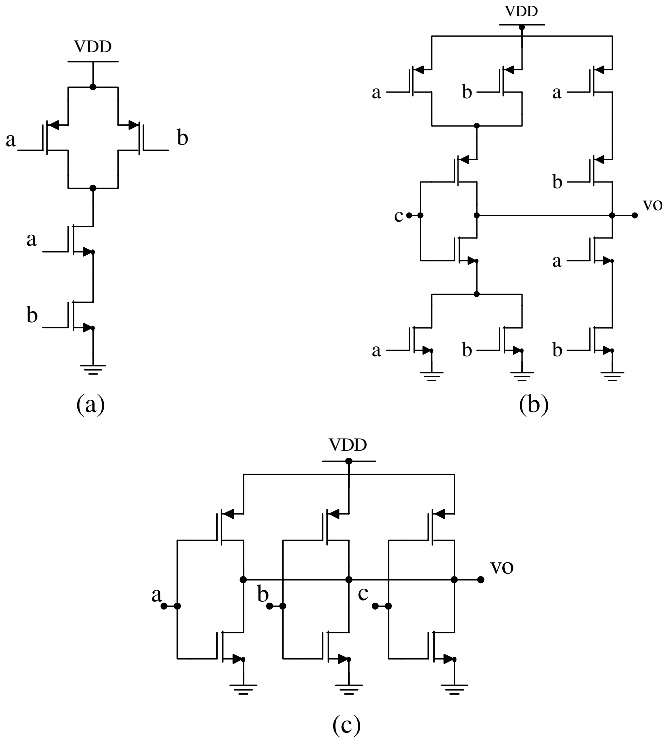

Fig. 1. CMOS gates: (a) static NAND-2; (b) mirrored MAJ-3; (c) output-wired MAJ-3

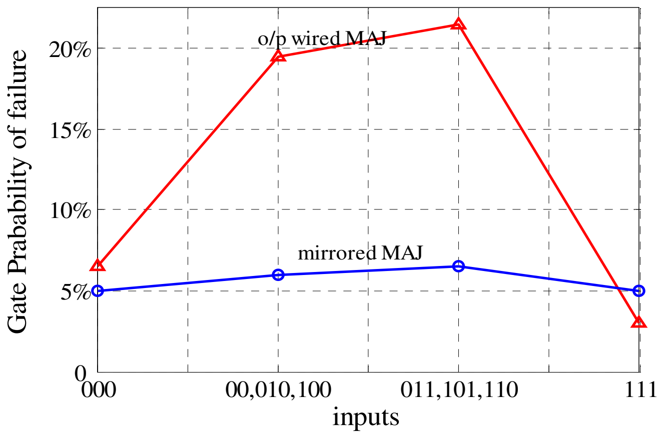

Fig. 2. Reliability of the mirrored MAJ-3 versus the output-wired MAJ-3

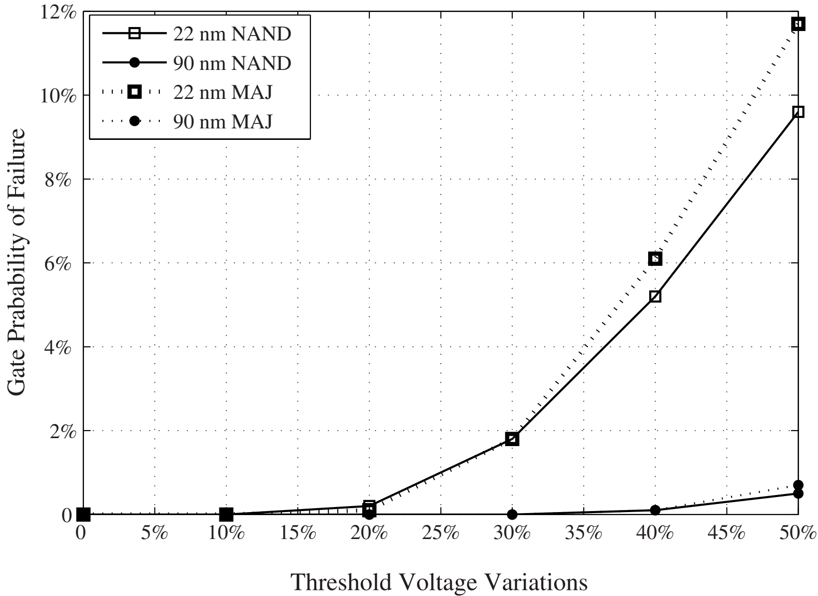

Fig. 3. Probability-of-failure (averaged over all input vectors) of the NAND-2 and MAJ-3

shows the results for the NAND-2 and the mirrored MAJ-3 gates at 90nm and 22nm.These results show that the gates can tolerate threshold voltage variations of up to 40% in 90 nm. This value is reduced to only 20% in 22nm technology. The results also show that the MAJ-3 is relatively similar to the NAND-2 in the 90nm technology. The difference between the two gates widens in 22nm when the threshold voltage variations are larger than 30%. Above this limit, the probability-of-failure of the MAJ-3 becomes larger than that of the NAND-2.

In order to get a clear insight on the behavior of these two gates, the probabilities of failures for the different input vectors have been investigated (Fig. 4 and Fig. 5). Fig. 4 shows the probability of failure of 22 nm NAND-2 for different inputs. The worst case is when both inputs are equal to 1. Here, the effect of threshold voltage variations on any NMOS may change the output. The best case is when both inputs are equal to 0, where the effect of threshold voltage variations on a single PMOS does not necessarily affect the output. Fig. 5 shows the results for the 22nm MAJ-3 gate. These reveal that the effects of the different input vectorss on the probability of failure is less significant, as compared to the NAND-2 gate case, especially at small variations. When considering the worst-case reliability of these two gates ('11' for the NAND-2, and '110/101/011' for the MAJ), we see that the MAJ-3 gate has a lower probability-of-failure than the NAND-2 for all variations (Figs. 4 and 5). This seems to contradict the results obtained with average values. However, this worst-case analysis gives more realistic results than the average-values analysis; hence, the MAJ-3 gate is more reliable than the NAND-2 at 22 nm.

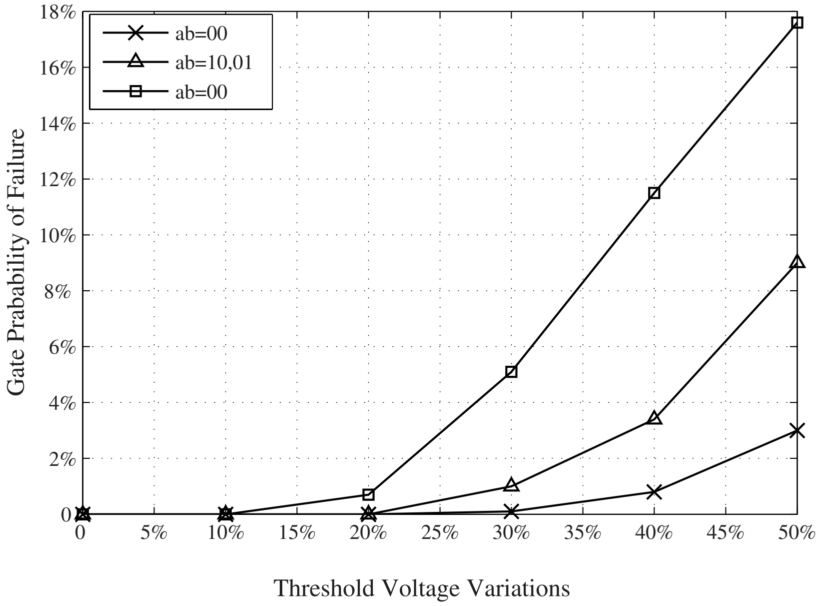

Fig. 4. Probability-of-failure of 22nm NAND-2

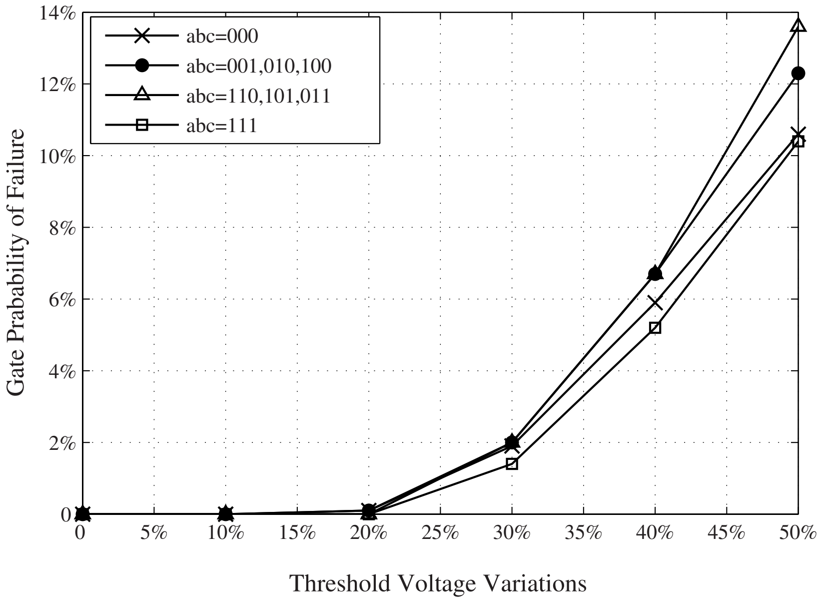

Fig. 5. Probability-of-failure of 22nm MAJ-3

These results are interesting because there has been ongoing debate (based mostly on theoretical analysis) about the robustness of the NAND and MAJ gates [14]. Since these two gates are the basic building blocks of the well-known multiplexing scheme ([1], [2]), it is important to evaluate the possible improvements in reliability that could be achieved with these schemes in the presence of threshold voltage variations. In order to evaluate these multiplexing schemes, it is important to also take into account the effect of interconnects' scaling, in addition to that of the gates. At the nanoscale, the smaller number of electrons will manifest both their discrete nature (which will modify their statistical behavior from the classical Gaussian towards a Poissonian one) and their quantum behavior (starting to show their wave-like part). The resulting statistical behavior on the wires [15] should be combined with the statistical distribution of the gate's threshold voltage variations to obtain more accurate estimates of any circuit (interconnected-gate scheme).

5 Conclusion

This study has investigated the effect of threshold voltage variations on the reliability of nanometer-scale CMOS logic gates. The reliability was quantified in terms of the probability-of-failure of individual gates, which was obtained from extensive Monte Carlo simulations. The study has considered the CMOS NAND-2 and MAJ-3 gates in two different technologies: 90nm and 22nm. The results show that these basic logic gates can tolerate up to 40% of threshold voltage variations in a 90nm technology, while only up to 20% in the 22nm technology node. The results also indicate that the two gates are equally reliable at 90nm, but the MAJ-3 seems to become more robust than the NAND-2 when moving to the 22nm. It is important to continue this investigation by integrating such results with system-level schemes for enhancing reliability (*e.g.*, multiplexing).

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