Ultra Low Energy Binary Decision Diagram Circuits Using Few Electron Transistors

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Abstract. Novel medical applications involving embedded sensors, require ultra low energy dissipation with low-to-moderate performance (10kHz-100MHz) driving the conventional MOSFETs into sub-threshold operation regime. In this paper, we present an alternate ultra-low power computing architecture using Binary Decision Diagram based logic circuits implemented using Single Electron Transistors (SETs) operating in the Coulomb blockade regime with very low supply voltages. We evaluate the energy – performance tradeoff metrics of such BDD circuits using time domain Monte Carlo simulations and compare them with the energy-optimized CMOS logic circuits. Simulation results show that the proposed approach achieves better energy-delay characteristics than CMOS realizations.

Keywords: low-energy circuits, singe electron transistors, binary decision diagram logic circuits.

1 Introduction

Technology scaling has lead to unprecedented level of integration with billions of nano-transistors on a single chip reducing cost per function. The exponentially increasing device density along with the supply voltage scaling hitting a plateau in traditional CMOS structures has made power consumption, the major design limiter. The ability to reduce the supply voltage is critical to the design of ultra-low power devices critical to the design of biomedical sensors that require long battery life time and low heat dissipation.

The electronics of a general biomedical sensor consist of energy delivery, analog-to-digital conversion, signal processing, and communication subsystems [1]. The design constraints for these individual components are intertwined. For example, for a given battery technology and size, reducing the signal processing power consumption from 10 mW to 8 μW can increase life time of the device from 3 days to 10 years between battery replacements [2]. The challenge of replacing batteries varies from being a nuisance as in external cochlear implants to surgical costs and inconvenience in case of implanted devices such as pacemakers. Consequently, a lot of attention is being focused on the use of energy scavenging techniques to power these biomedical sensors. The human body itself can be a source for scavenging energy. The heat flow generated by the human body has a power density of approximately 20mW/cm2 on

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average [3] and serves as a good source of thermal energy. Another research direction in energy scavenging is to harvest hydraulic energy in the human body, including blood flow, heart beats, and contraction of blood vessels [1]. While these energy scavenging schemes are attractive options to eliminating the need for batteries, they have limited power generation ability. For example, a wrist-watch type thermoelectric generator can generate a useful power of 0.2-0.3 mW in average based on normal human activity [3]. Consequently, the trend towards adopting energy harvesting designs accelerates the need for ultra-low power systems.

While power reduction is critical for all the components of a biomedical sensor, the focus of this work is on design of ultra-low power signal processing fabric. We present a ultra-low power computing architecture using Binary Decision Diagram based logic circuits implemented using Single Electron Transistors (SETs) operating in the Coulomb blockade regime with very low supply voltages (150 to 75 mV). These low operating voltages not only enable ultra-low power devices but also bring the signaling voltages close to those found in biological neuron systems. In this paper, we present an ultra-low power computing architecture using Binary Decision Diagram based logic circuits implemented using Single Electron Transistors (SETs) operating in the Coulomb blockade regime with very low supply voltages. We evaluate the energy – performance tradeoff metrics of such BDD circuits using time domain Monte Carlo simulations and compare them with the energy-optimized CMOS logic circuits. Simulation results show that the proposed approach achieves better energy-delay characteristics than CMOS realizations and is an attractive candidate for implementing low-energy biosensor digital processing circuits.

2 Background and Related Work: SET Circuits

The inhibition of current flow across a nanoscale island, which is isolated via high resistance tunneling barriers, when a small bias voltage is applied, is termed as Coulomb Blockade. This phenomenon which was observed several decades ago was observed to occur when the self charging energy e^2/C_Σ of a nanoscale island of capacitance C_Σ exceeds the thermal energy K_BT and when the tunnel barrier resistance R_T exceeds the quantum of resistance, $R_H = h/e^2$ (26 k(). Under these conditions, a Coulomb Gap arises in the nanodot which can be exploited to build Single Electron Transistors (SETs) or to build Single Electron Pumps which can be used to perform controlled transfer of electrons. The low power consumption of single electron transistors arises primarily from carriers tunneling through high resistance tunnel barriers (of the order of mega-ohms) typically under very low supply voltages (of the order of milli-volts) leading to drive currents in the scale of nano-amperes. This low current drivability of SETs also makes it challenging when interfacing with CMOS circuit applications.

Single electron tunneling phenomena are particularly interesting in the era of modern nanoscale devices mainly because of the fact that as the island dimensions shrink, the self charging energy of the island with capacitance C_Σ, given by e^2/C_Σ increases, and it is possible to observe Coulomb Blockade at room temperature. There have been research publications which detail the observation of Coulomb Blockade phenomena at room temperature [4] [5]. Thus, there is significant interest

in SET circuits because this gives rise to the possibility of implementing ultra-low power circuits using nanoscale devices which are capable of gigascale integration and operation at room temperature.

There have been numerous fabrication efforts to develop conducting islands which are connected to the external environment through tunnel barriers. Notable fabrication developments are Pattern Dependent Oxidation (PADOX) and Vertical-Pattern Dependent Oxidation (V-PADOX) [6] where structure dependent stress patterns that occur during the thermal oxidation of silicon structures are exploited to isolate a silicon island separated by tunnel barriers. Another noteworthy fabrication effort is the fabrication of Binary Decision Diagram based SET circuits using Selective Area Metal-Organic Vapor-Phase Epitaxy (SA-MOVPE) technique on GaAs substrates [7, 8, 9].

The orthodox theory of single electron phenomena which matured during the mid 80s [11, 12, 13] is an energy based model which utilizes the change in the free energy of the system due to various tunneling events to compute the probability rates for the same. The rate equations can then be used to either obtain a closed form analytical solution for the current-voltage characteristics [14] or to perform Monte-Carlo simulation of the tunneling activity. This energy based model lead to the development of many simulation tools [15, 16, 17, 18], SIMON [18] being one of the more widely-used tools.

Following the development of simulation tools for single electron phenomena, there have also been numerous circuit design efforts. Most of such circuits can be classified either as based on Single Electron Logic or based on Single Electron Transistor Logic. Single Electron Logic circuits work by using a single electron to capture a bit of information. Quantum Cellular Automata or phased-clock controlled BDD type circuits are good example of circuits which use Single Electron Logic. Single Electron Transistor Logic circuits [21,22,23] on the other hand resemble CMOS circuits and utilize voltage levels on output load capacitances in order to denote a logic level.

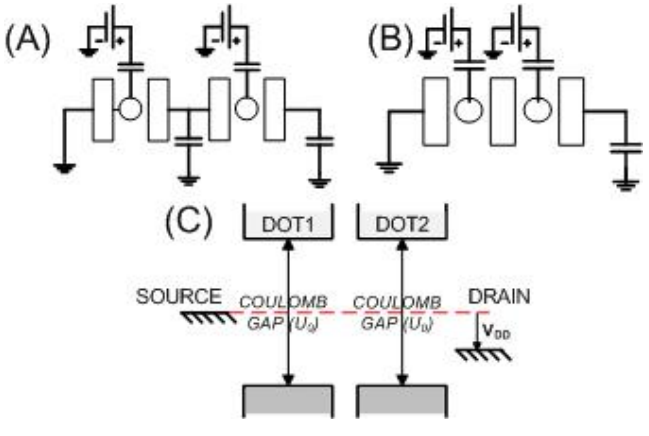

Fig. 1. a) SET transistors in series. b) Coupled nanodots. c) Band diagram of coupled SET nanodots.

When SET Logic circuits are designed to mimic CMOS circuits (for example, as shown in Figure 1 A), simulations show that such circuits tend to have poor performance [21,22,23]. This is mainly because of the inherently low drive current strength of SETs (due to the high resistance tunneling barriers) and because of the parasitic capacitances that result from the conducting wires that is used to connect the SETs in series. It is to be noted that source/drain parasitic capacitances in CMOS design are unavoidable due to the nature of CMOS transistors and in the case of SET circuits, the wires that are used to make connections between series SETs give rise to parasitic capacitances. In order to improve performance, some SET circuit models have been proposed in the literature that use multi-gate designs [23, 24].

3 Proposed Coupled Nanodot SET Circuits

We utilize a coupled nanodot array where the parasitic load capacitances around individual SETs at each node are eliminated as shown in Figure 1 B. In such a device, the band structure of the nanodots is still preserved due to the poor coupling (captured as the tunneling resistance R_T) between the nanodots [20]. However, due to the self charging energy there is still a Coulomb Gap present in both the nanodots as shown in Figure 1C. When only one nanodot is turned on by applying a voltage of $e^2/2C_G$ (charging energy of a quantum dot of capacitance C) + $V_D/2$ (supply voltage) to a control gate as shown in Figure 2A, no current flows across the device. Only when both the SETs are turned on as shown in Figure 2B, there is a current across the device allowing the load capacitance to charge up.

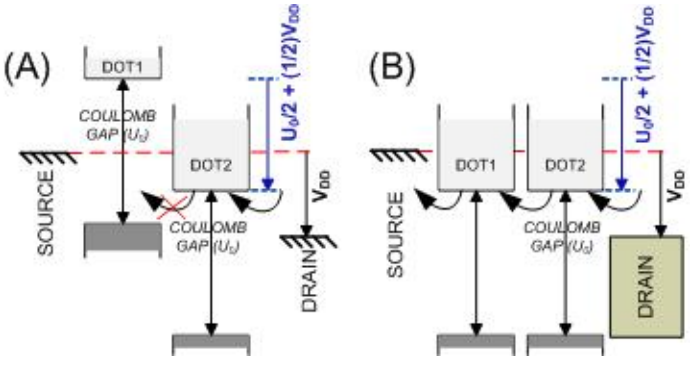

Fig. 2. a) Band structure of series SETs when the first nanodot is turned on. b) Band structure when both nanodots are turned on.

To exploit this controlled dot-to-dot tunneling to realize other circuits in a systematic manner, we use a binary decision diagram (BDD) based logic architecture. Traditionally, BDDs have been used as a data structure in CAD tools and is an attractive option in our case as it avoids high fan-out structures. A BDD is a directed graph and an alternate representation of the truth table. Any combinational logic can be built using BDD. Consider the following example of a 2-bit comparator which compares 2 two-bit binary numbers A and B and outputs [01] if A < B, [10] if A > B and [00] if A=B. The implementation using NAND gates is shown in Figure 3A.

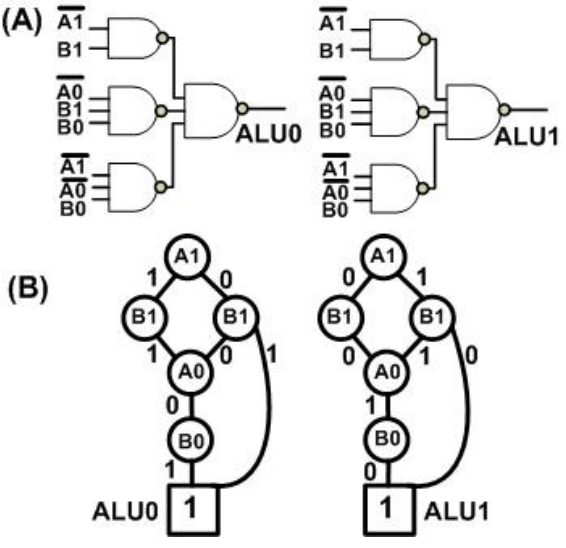

Fig. 3. a) NAND gate based implementation of 2 bit comparator. b) Binary Decision Diagram of 2-bit comparator.

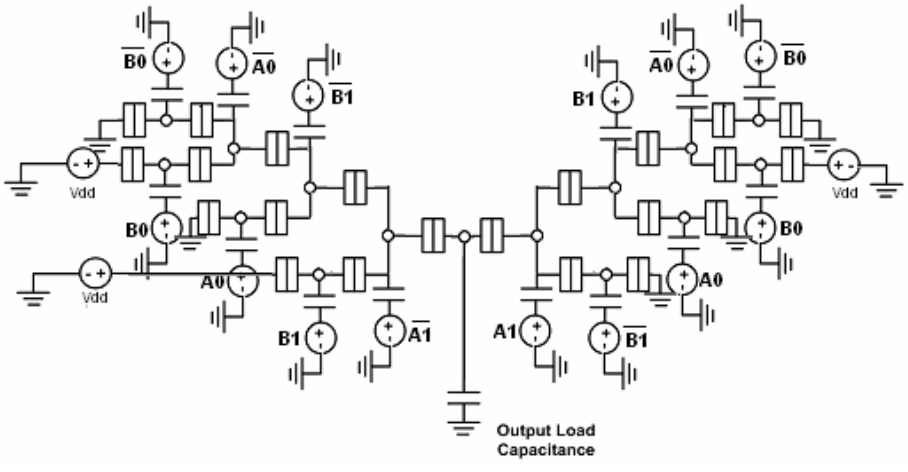

Fig. 4. Implementation of BDD of 2-bit comparator circuit using SET nanodots

The BDD of the 2-bit comparator is shown in Figure 3B and the schematic of an implementation of the BDD using closely coupled SET nanodots is shown in Figure 4. Due to the intrinsic topology of a BDD, each nanodot is coupled to at most two nanodots coming from above or to at most two nanodots from below. In the implementation shown in Figure 4, the output V_D is lower than the gate voltage required to drive the next stage of the logic, a restoring latch, which takes a supply voltage V_D as input and outputs a voltage equal to $U_0/2 + V_D/2$. We realize other circuits in SET logic in a similar fashion using the BDD representation.

4 Experimental Evaluation

We implemented three arithmetic circuits: a XOR gate, a 2-bit adder and a 2-bit comparator using SET logic. These circuits were simulated using SIMON 2.0, a Monte-Carlo simulator at room temperature. While SIMON assumes charge quantization on each individual quantum dots, due to high barrier resistance, the simulation on the ensemble of the quantum dots in the circuits is equivalent to the quantum assessment of the entire system [25, 26]. For these experiments, the gate capacitance (C_G) was set to 0.3aF to provide a desired ratio of 10 between the charging energy of the nanodot (e^2/C_G) and the thermal energy at room temperature (k_BT). The ratio of the tunnel barrier capacitance to the gate capacitance was set to 0.1 through experimentation to improve noise margin and off-state leakage. Finally, the tunnel barrier resistance in our experimentation was 1 MΩ.

We analyzed the delay and energy consumption for these circuits by varying the supply voltage from 150mV to 75mV. Delay is defined as the time required for the output to reach 90 % of the supply voltage. Since tunneling is a probabilistic phenomenon, we compute a distribution for the delay through simulation and report the average. The energy is measured by tracking the charge drawn from the supply voltage during the given interval and is also an average. A representative delay and energy distribution for a XOR gate operating at 100 mV is given in Figure 5A and 5B.

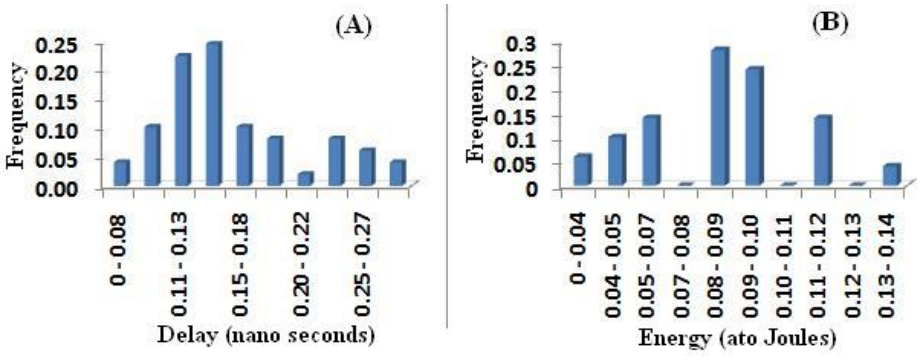

Fig. 5. a) Delay distribution for a BDD Xor circuit operating at 100 mV. b) Energy distribution for a BDD Xor circuit operating at 100 mV.

We observe that the BDD circuit can employ aggressive voltage scaling and still be functional. Our analysis (Figure 6A) shows that the energy for an XOR circuit (when driving a 10 aF load capacitance) reduces from 0.22 aJ (150 mV) to 0.04 aJ (75 mV) without a significant degradation in performance (Figure 6B) when scaling supply voltage. In comparison, for an XOR gate realized in 32 nm CMOS when the supply voltage is swept from 150mV to 120mV, the energy first reduces slightly from 8 aJ and then increases to 12 aJ due to increased leakage energy as shown in Figure 7 (The energy profile for XOR implemented using SET nanodots is shown for comparison). It must be observed that the SET realization provides an order magnitude benefit in energy. Further, the delay of CMOS circuit degrades significantly with supply voltage

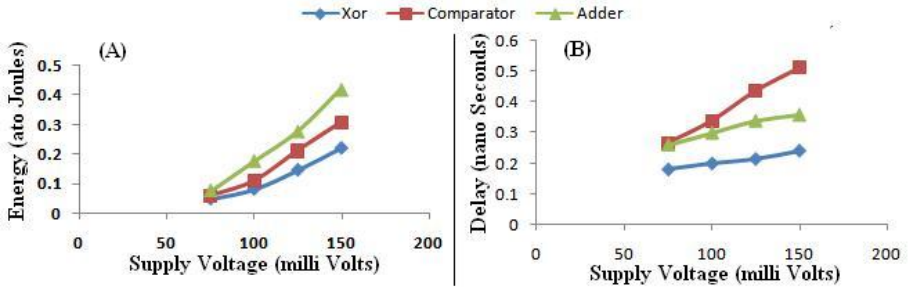

Fig. 6. a) Energy trend for SET implementations of Xor, comparator and adder circuits. b) Delay trend for SET implementations of Xor, comparator and adder circuits.

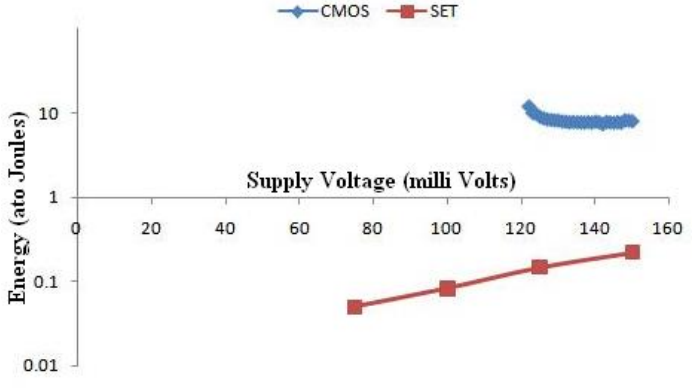

Fig. 7. Energy trend for CMOS implementation of Xor function and comparison with the energy trend for SET implementation

reduction. The energy-delay trends for the SET implementations of the comparator and adder circuits are also shown in Figure 6A and 6B.

Next, we evaluate the energy-performance tradeoff of the SET circuit, in case the BDD-logic needs to interface with traditqional CMOS circuit. Such an interface is also essential when one SET stage drive the gates of the next SET stage which requires a higher voltage ($e^2/2C_G + V_D/2$) than the supply voltage (V_D). To evaluate this scenario, we included a level converter implemented as a cascade of two inverters at the output of the SET circuits. Further, we experimented with different activity factors for the designs to compare with the corresponding CMOS implementations. We used complementary CMOS logic to implement the example circuits, also using the stacking effect to minimize leakage where possible. For the CMOS implementations, we identified the minimum energy combination of supply voltage and threshold voltage for each of the activity factors. We used a method of supply voltage and threshold voltage scaling as studied in [27] in order to determine the minimum energy point for the CMOS implementations done in 32 nm technology. Our results indicate that our SET designs have comparable energy consumption to CMOS implementation while providing significantly better performance. Consequently, they exhibit much lower

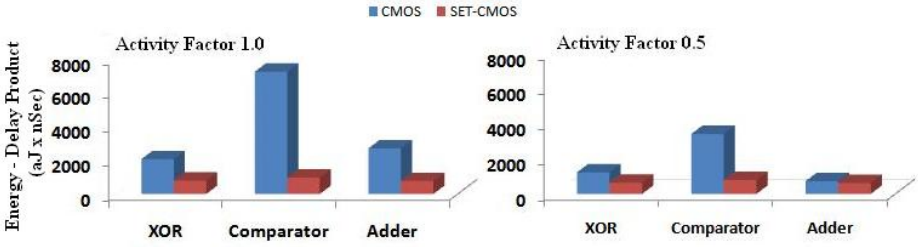

Fig. 8. Energy-Delay product comparison for CMOS implementation and SET-CMOS implementation of Xor, comparator and adder for Activity Factor 1.0 and Activity Factor 0.5

energy-delay product (Figure 8) than their CMOS implementations. It should also be observed that our SET-CMOS parameters were not customized for each circuit for different activity factor unlike CMOS.

4 Conclusion

Ultra-low power signal processing will be critical to the design of next generation biomedical sensors. In this work, we have demonstrated a novel realization of the BDDs of simple logic circuits, like Xor, Comparator and Adder, using coupled nanodots. We have demonstrated that these circuits can operate at very low supply voltages in the range of 150 to 75mV at room temperatures. Our results also show that these devices consume very low energy and provide better performance than energy-optimized CMOS circuits. Consequently, these devices may be good candidates for implementing signal processing circuits in next generation sensors.

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