Designing Reliable Digital Molecular Electronic Circuits

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Abstract. Reliability is expected to be a critical challenge in designing future molecular electronic circuits. Using a compact model that captures the essential physics of the device, the effect on digital gate functionality of variations in the device parameters, as well as the improvements afforded by a TMR majority gate structure are quantified. It is shown that the improvement is substantial, showing the potential viability of such technologies in future massively integrated systems.

Keywords: molecular electronics, circuit simulation, nanotechnology.

1 Introduction

[1] Electronic molecules serving as active elements in future nanoelectronic circuits have received a wealth of attention recently [1,2,3]. As these devices work at very low energy levels approaching thermal energy limits, they exhibit very noisy characteristics. For reliable information processing using such molecular circuits in the presence of noise, the development and adaptation of classical fault tolerant structures for nanoscale circuits becomes essential. Fault tolerance for nanoelectronic circuits has been studied at an abstract level [4,5] but it is desirable to quantify the performance of actual circuits in order to get a measure of the feasibility of using nanoscale non-classical devices in electronic applications. In such a study, it is desirable to capture the quantum level physical behavior of the devices as accurately as possible, within the constraints imposed by the computational complexity of the model.

Previously, we have proposed a compact model to describe a class of devices with two terminals where the dominant current transport mechanism is resonant tunneling [6]. This model, which consists of an extension to the Breit-Wigner (BW) formula to describe the dynamic behavior of the device, captures the essential physics of the device while being computationally efficient enough to explore the behavior of relatively large circuits in multiple configurations. In this paper, we use this compact model to demonstrate digital functionality with molecular devices within a regular matrix of nanowires that has been proposed as an architecture for future massively integrated nanoelectronic systems [7]. Building on previous work [8] we show how the device is vulnerable to variations in

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physical quantities which translate to realistic fabrication tolerances, and quantify their effect on circuit behavior using accepted digital quality metrics. We then explore the efficacy of a classical error tolerant structure, triple modular redundancy (TMR) with a majority gate in coping with these variations, and ensuring circuit behavior within prescribed noise and delay margins. The rest of this paper describes the device model in section 2, and the circuit simulations and results in section 3. We end with our conclusions.

2 Device Model

The device model is briefly described in this section; detailed descriptions can be found in [6]. The integral equation

$$I_0(V) = \frac{2e}{h}\int_{\infty}^{\infty} dE \frac{4\Gamma_1\Gamma_2[f(E-\mu_s) - f(E-\mu_d)]}{[(E-\epsilon_0)^2 + (\Gamma_1+\Gamma_2)^2]}. \quad (1)$$

describes the current through the molecule as a function of the voltage across it. Γ_1 and Γ_2 represent the coupling of the molecule to the leads and ϵ_0 gives the position of the resonance peak (Figure 1a).

The coupling factors Γ_1 and Γ_2 can also be used to describe the difference between the time spent by the electron in the region of the scattering interaction and the time spent in the same region in the absence of the scattering interaction to build the dynamic extension to the device model. The full device characteristic is given in:

$$I_{DS}(t) = I_0(1 - exp(\frac{-t(\Gamma_1+\Gamma_2)}{\hbar})). \quad (2)$$

The equivalent circuit of the model is shown in Figure 1b. It has two main parts: a complex diode with I-V characteristics given by (1) to model the static or

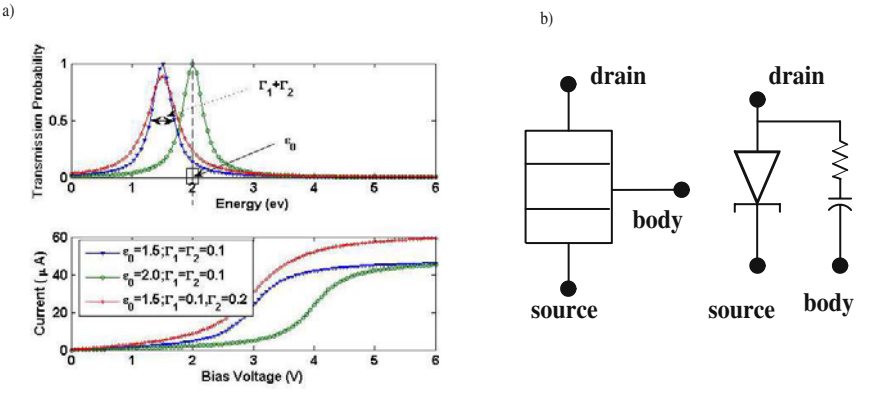

Fig. 1. a) The transmission probability as a function of molecular energy and corresponding $I-V$ characteristics for different coupling parameters b) equivalent circuit for the full device model

steady-state current, and a capacitor to model the exponential growth/decay of charge that takes place in the accumulation of electrons on the molecule. The third terminal is assumed to be implicitly connected to signal ground in a two-terminal configuration.

3 Implementation and Results

The general form of a molecular gate in a cross-bar architecture [7] is a complex network of molecules with pull-up and pull-down resistors, where the input vector is on the row wires and the output is presented vertically on the column wires [3,9]. A representative example, a two-input AND gate, is shown in Figure 2a. The rail voltage Vdd is set to 1V based on the separation between the lowest high output and the equivalent thermal noise related voltage at the operating temperature, around 6mV at room temperature. The separation between low and high values is a critical metric in digital logic, and is defined here as the noise margin.

Due to the inherently poor control over nano-fabrication techniques, it is difficult to form identical molecular junctions, fundamentally affecting device characteristics and essentially rendering some devices unusable. Statistical variation in electrical properties of low-dimensional conductors can arise from random variations along the length of the conductor [10,11], from disorder in the substrate and from variations in the distance between the substrate and the molecular anchors groups. Figure 2b shows the variation of the noise margin with the primary physical characteristics of the device, the value of ϵ_0 representing an internal energy and $\Gamma_1 = \Gamma_2 = \Gamma$ representing the coupling of the device to the leads. As can be seen, when a large value of ϵ_0 coincides with a small value of Γ, the noise margin of the AND gate falls below $0.2V$ and the gate fails.

As a result, this essentially means that some portion of the gates on a chip will be unusable. Along with some percentage of the devices never working at all, a likelihood exists that some of the devices will work some of the time. This is potentially a bigger problem leading to intermittent system failures. The solution to this problem is more likely to be found in the architecture of the system. Most fault-tolerant techniques for nanocomputing feature some sort of redundancy. The basic idea is that a function is implemented many times, and the output is resolved through a majority gate. So for example, if the redundancy is a factor of three, and each block should output logic 1, but due to an error only two function correctly, the output is proportional to 2/3 rather than 1. By relaxing the threshold appropriately, the correct output can still be obtained. In Figure 2c and 2d respectively, the circuit of a majority gate with n redundacy using molecular devices and a resistor and the fault-tolerant construction of an AND gate are shown. The output of the majority gate is equal to the sum of the input voltages divided by n if the resistance of the resistor is much bigger than the equivalent resistance of the molecular devices. The performance of the TMR gate can be investigated by running Monte Carlo simulations over distributions of the physical parameters, representing manufacturing variations. The noise

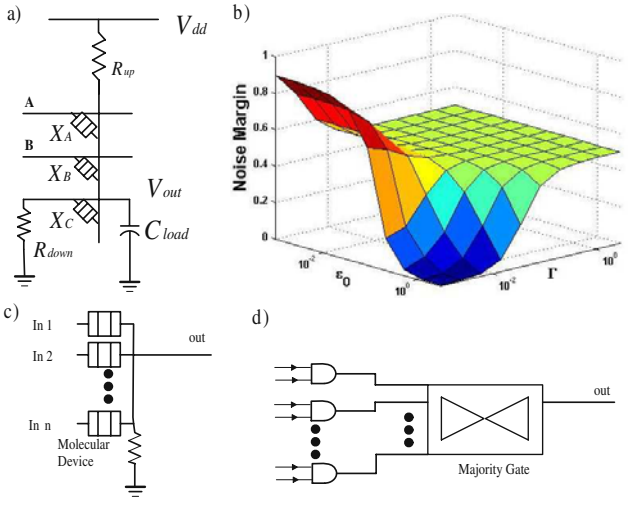

Fig. 2. a) Circuit layout for the AND gate; b) variation of the noise margin of the AND gate with Γ and ϵ_0; c) circuit layout for the majority gate; d) n-redundant construction of AND gate using molecular devices

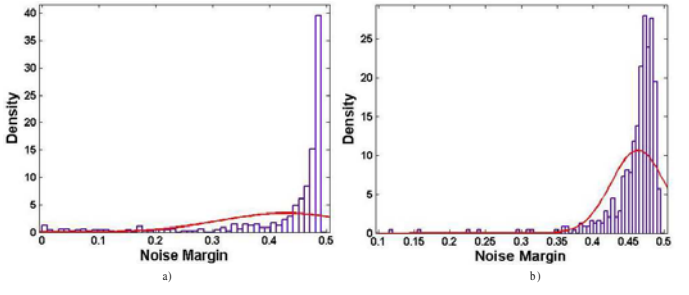

Fig. 3. a) Density distribution for the noise margin of the AND gate; b) density distribution for the noise margin of the fault-tolerant AND with with a uniform distributions for Γ (ranging from 0.0001 to 0.1999) and ϵ_0 (ranging from 0.1 to 2.9), $R_{down} = 10M\Omega$ and $C_{load} = 10aF$

margin of a molecular AND gate and its fault-tolerant construction are shown in Figure 3a and 3b. In this simulation 500 iterations were carried out with the parameters Γ and ϵ_0 assumed to be uniformly distributed with mean values $\Gamma = 0.1eV$ and $\epsilon_0 = 1.5eV$. Assuming a noise margin below $0.3V$ to constitute failure, the failure probabiliy has dropped from 1.1% to 0.1%.

4 Conclusions

The viability of future molecular electronic systems depends firmly on their reliability. In this work we have used a compact device model that captures the

essential quantum mechanical behaviour of a class of molecules to quantify the reliability of molecular circuits within a realistic architecture, in the face of variation in device characteristics that can be expected from typically poor control over nano manufacturing techniques. We have investigated the performance of the classical TMR majority gate structure when the majority gate itself is constructed from imperfect devices and shown that gate-level reliability can be significantly increased. While the improvement obtained for this particular example (up to 99.9%) falls short of approaching the reliability of current high volume production CMOS processes, the amount of redundancy can be increased to further improve reliability, at little area cost given that all gates are constructed from molecular devices. These results suggest a means of overcoming the limitations of stochastically unreliable molecular devices through redundancy based strategies, highlighting the potential of such future technologies.

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