# Functional Model of Carbon Nanotube Programmable Resistors for Hybrid Nano/CMOS Circuit Design

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**Abstract.** Hybrid Nano (e.g. Nanotube and Nanowire) /CMOS circuits combine both the advantages of Nano-devices and CMOS technologies; they have thus become the most promising candidates to relax the intrinsic drawbacks of CMOS circuits beyond Moore's law. A functional simulation model for an hybrid Nano/CMOS design is presented in this paper. It is based on Optically Gated Carbon NanoTube Field Effect Transistors (OG-CNTFET), which can be used as 2-terminal programmable resistors. Their resistance can be adjusted precisely, reproducibly and in a non-volatile way, over three orders of magnitude. These interesting behaviors of OG-CNTFET promise great potential for developing the non-volatile memory and neuromorphic adaptive computing circuits. The model is developed in Verilog-A language and implemented on Cadence Virtuoso platform with Spectre 5.1.41 simulator. Many experimental parameters are included in this model to improve the simulation accuracy.

**Keywords:** Functional Modelling, Carbon Nanotube, Hybrid Nano/CMOS circuits, OG-CNTFET, Verilog-A.

## 1 Introduction

Nano-devices with amicable interface with CMOS technology (e.g. Nanotube and Memristor) [1-4] are of great interest to relax the intrinsic drawbacks of CMOS technology and improve furthermore the circuit performances beyond the Moore's law. These hybrid Nano/CMOS circuits promise to combine both the advantages of Nano-devices and CMOS technology [2]. In order to develop the hybrid circuits and architectures, the functional spice simulation model of Nano-devices is required as it can provide the interface between the physical behaviours of the Nano-devices and electrical test-bench. By using the functional model and CMOS design kit, the performance of these hybrid circuits can be simulated before the prototyping and the architecture comprising hundreds or thousands nano-devices can be also predicted. Different from the compact model [3] which is used often for the basic circuit design, functional model promises much higher simulation speed and it allows also the designers to ignore the undesired physical phenomena.

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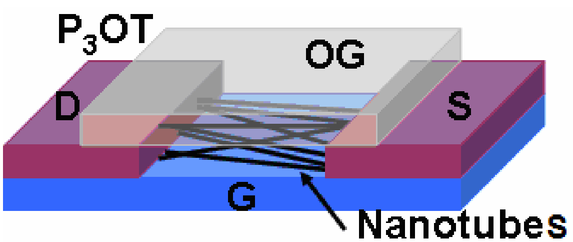
In this paper, we present the functional model of Optically Gated Carbon NanoTube Field Effect Transistors (OG-CNTFET) [1], which can be used as 2-terminal programmable resistors and promise great potential for the non-volatile memory and neuromorphic adaptive computing applications. The model is programmed with hardware description language Verilog-A and the hybrid simulation platform is Cadence Spectre 5.1.41.

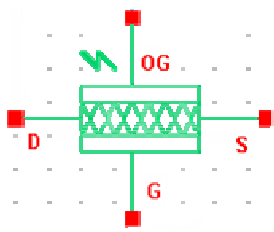
## 2 Functional Model of OG-CNTFET for Hybrid Circuit Design

### 2.1 Physical Structure of OG-CNTFET and Its Spice Symbol

There are four terminals in the OG-CNTFET (see Fig.1), Drain (D), Source (S) and Gate (G) as the conventional CNTFET [4] and an additional Optical Gate (OG) allowing the electrons to be trapped below the nanotube network. In practical applications, the terminals G and OG are shared by a number of OG-CNTFETs. The other two terminals D, S form the tunable resistance $R_{DS}$, which can be adjusted precisely, reproducibly and in a non-volatile way, over three orders of magnitude [1].




(a)




(b)

**Fig. 1.** (a) Physical structure of OG-CNTFET is composed of four terminals (b) Symbol of OG-CNTFET in the schematic editor Spectre of Cadence

### 2.2 Switching Behaviors and Equivalent Electrical Circuits

The model integrates both the switching behaviors of OG-CNTFET from “off” to “on” state and the reverse. The resistance ($R_{DS}$) between the source and the drain returns to $R_{on}$ from any other state by exposing the OG-CNTFET to a laser beam pulse at an appropriate wavelength (e.g. $\lambda$=457nm). Multi-level resistance can be generated if the duration of the laser pulse is short enough. $R_{DS}$ can be reset to any higher resistance up to $R_{off}$ by applying a positive voltage pulse at drain ($V_D$). $R_{off}$ depends only on the amplitude of $V_D$, but the reset path showing multi-level depends on both the amplitude and the pulse duration of $V_{D.}$ Equation 1 describes the evaluation of resistance reset path (I) with the time axis (x); all the other factors ($x_0$, $y_0$, $A_{1\text{-}3}$, $b_{1\text{-}3}$) are constants calculated directly from the experimental measurements for a given $V_D$, for example, as $V_D$= 5V, the constants are respectively $X_0$=2.15497e-11,

$Y_0$=9.48e-3, $A_1$=4.0801e-1, $A_2$=4.0801e-1, $A_3$=1.4646e-1, $b_1$=1.5957e-1, $b_2$=1.1596e-1, $b_3$=1.00955. The precise factors allow high accuracy simulations and the difference between the simulation results and experimental data could be lower than 3%.

Based on the switching behaviors of OG-CNTFET, equivalent electrical circuits have been implemented in the model (see Fig.2). $R_0$ and $R_1$ forming the $R_{on}$ are constants obtained from the experimental measurement. $R_A$ and $R_B$ are tunable resistances from 0 to $R_{off}$. $V_{OG}$, n and t represent the wavelength of laser, number of pulses and the pulse duration respectively.

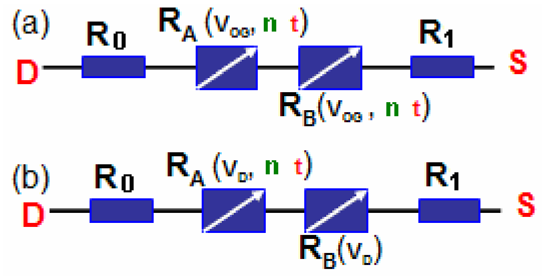



**Fig. 2.** (a) Equivalent circuit of OG-CNTFET from the "off" to "on" state, $R_A$ and $R_B$ are tunable resistance and depend dynamically on the duration of laser. (b) Equivalent circuit from "on" to "off" state, $R_B$ depends on only the drain voltage and $R_A$ varies dynamically with the drain and gate voltage.

$$I = y_0 + A_1 \times \exp(-\frac{(x-x_0)}{b_1}) + A_2 \times \exp(-\frac{(x-x_0)}{b_2}) + A_3 \times \exp(-\frac{(x-x_0)}{b_3}) \qquad (1)$$

This functional model provides high flexibility for hybrid Nano/CMOS design; the configuration of $V_D$ can be changed to get the desired results. For example by lowering the pulse duration, more resistance states can be obtained and then improve the circuit precision; by improving the $V_D$ amplitude, there will less resistance states but the circuit speed can be accelerated. The best design could be the tradeoff between speed and precision with the most suitable $V_{D.}$ Spice simulations have been done after the implementation of the electrical equivalent circuit in the Verilog-A model. Fig.3 shows the programmable resistivity of OG-CNTFET driven by both the laser (from $R_{off}$ to $R_{on}$) and $V_D$ (from $R_{on}$ to $R_{off}$). Fig.4 shows different reset paths of OG-CNTEFT led by the three $V_D$ amplitudes, this effect can be explained by the resistivity ($R_B$) during the reset path (see Fig.2b), which depends only on the amplitude of $V_D$.

### 2.3 Intrinsic Random Initial Effect of Nanocomponents

The small dimension of nanocomponents and their self-assembly fabrication process leads to intrinsic important process and mismatch variation, which could have critical influences on the hybrid circuits and architecture design [7]. Thereby the random initial effect has been taken into account in the functional model to improve the simulation accuracy and reliability (see Fig.5). Based on our experimental measurement,

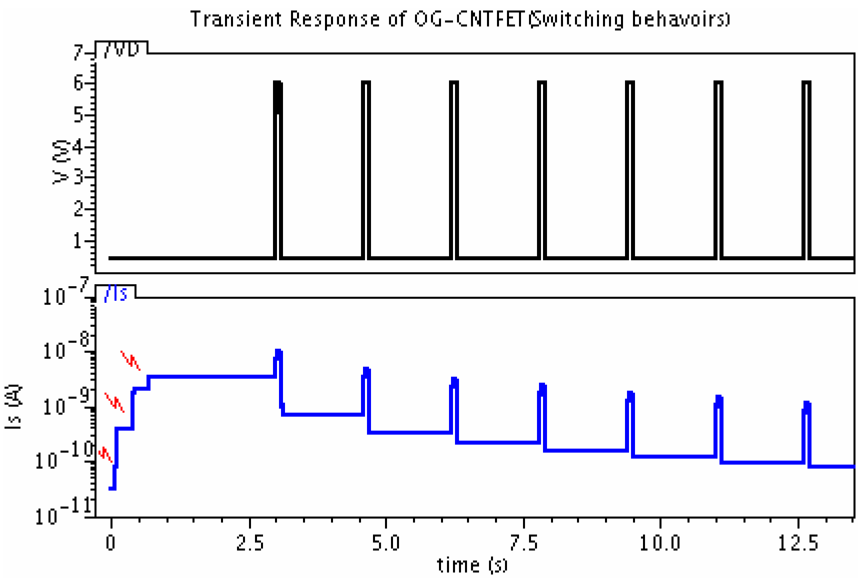



**Fig. 3.** Spice simulation of OG-CNTFET functional model. Three laser pulses (red flashes) are used here to drive it from "off" to "on" state. The VD pulse (100ms@6V, 0,4V) reset the OGCNTFET from "on" to "off" state.

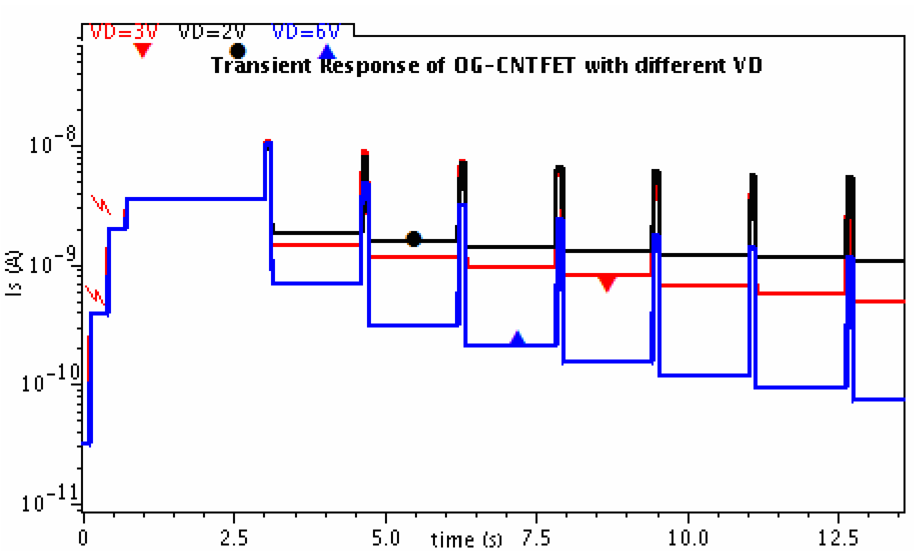



**Fig. 4.** Spice simulation of OG-CNTFET functional model, three laser pulses drive it from "off" to "on" state. Different VD pulse (100ms@2, 3 and 6V, 0.4V) reset the OGCNTFET from "on" to "off" state in different path. As mentioned, the Roff resistance depends on the amplitude of VD.

the random initial state of different OG-CNTFETs is found to follow approximately the Gaussian distribution and the maximum resistance variation is about 23.68% [1]. This effect is useful to demonstrate the robustness and reliability of the hybrid circuits and computing architectures under development in our group.

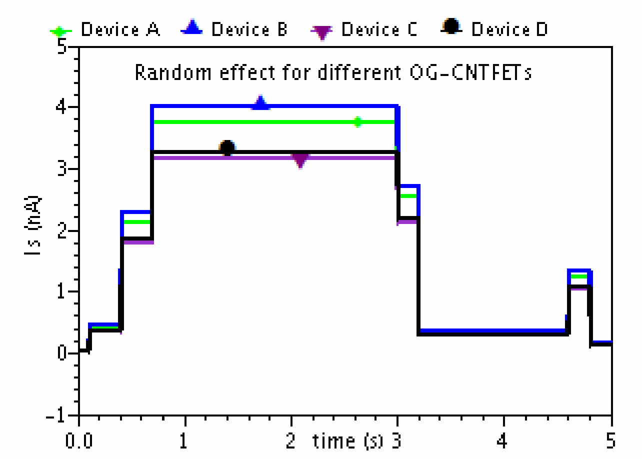



**Fig. 5.** The initial state of the OG-CNTFET functional model is random and based on the Gaussian distribution measured from the experiments

## 3 Conclusions

This paper introduces a functional model of OG-CNTFET for hybrid Nano/CMOS design; it includes the dynamic behaviors, random initial effect and a number of experimental parameters. The structure of this functional model could be easily used to develop functional models for other two terminals programmable nanocomponents such as CBRAM [5] and NOMFET [8] Memristor [9] etc. Based on this model and CMOS 65nm design kit [10], hybrid neuromorphic circuits comprising nanoscale synapses and CMOS neurons are under investigation in our laboratory [11].

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## References

1. Borghetti, J., Derycke, V., Lenfant, S., Chenevier, P., Filoramo, A., Goffman, M., Vuillaume, D., Bourgoin, J.P.: Optoelectronic switch and memory devices based on polymer-functionalized carbon nanotube transistors. Advanced Materials, 2535–2541 (2006); (b) Agnus, G., et al.: Carbon Nanotube Programmable Resistors. Advanced Materials (2009) (Submitted)

2. Strukov, D.B., Likharev, K.K.: CMOL FPGA:a reconfigurable architecture for hybrid digital circuits with two-terminal nanodevices. Nanotechnology 16, 888–900 (2005)
3. Liao, S., Maneux, C., Pouget, V., Fregonese, S., Zimmer, T.: Compact modelling of optically-Gated Carbon Nanotube Field Effect Transistor. Trends in Nanotechnology (2009)
4. Javey, A., Guo, J., Wang, Q., Lundstrom, M., Dai, H.J.: Ballistic carbon nanotube field-effect transistors. Nature 424, 654–657 (2003)
5. Dietrich, S., Angerbauer, M., Ivanov, M., Gogl, D., Hoenigschimid, H., Kund, M., Liaw, C., Markert, M., Symanczyk, R., Altimime, L., Bournat, S., Mueller, G.: A Non-volatile 2-Mbit CBRAM Memory Core Featuring Advanced Read and Program Control. IEEE Journal of Solid-State Circuits 42, 839–845 (2007)
6. Verilog-A Language Reference Manual, Agilent Technologies (2004)
7. Lu, W., Lieber, C.M.: Nanoeletronics from the bottom up. Nature Materials 6, 841–850 (2007)
8. Novembre, C., Guerin, D., Lmimouni, K., Gamrat, C., Vuillaume, D.: Gold nanoparticle-pentacene memory transistors. Applied Physics Letters 92, 103–314 (2008)
9. Strukov, D.B., Snider, G.S., Stewart, D.R., Williams, R.S.: The missing memristor found. Nature 453, 80–83 (2008)
10. STMicroelectronics, Design Rules Manuel, 65nm low power (2008)
11. Zhao, W., Gamrat, C., Agnus, G., Derycke, V., Bourgoin, J.P.: Neural network circuit comprising nanoscale synapses and CMOS neurons, European Patent Number 09305240.5 (2009)