Through Silicon Via-Based Grid for Thermal Control in 3D Chips*

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Abstract. 3D stacked chips have become a promising integration technology for modern systems. The complexity reached in multi-processor systems has increased the communication delays between processing cores, and an effective way to diminish this impact on communication is the 3D integration technology and the use of through-silicon vias (TSVs) for inter-layer communication. However, 3D chips present important ther- mal issues due to the presence of processing units with a high power density, which are not homogeneously distributed in the stack. Also, the presence of hot-spots creates thermal gradients that impact negatively on the system reliability and relate with the leakage power consumption. Thus, new approaches for thermal control of 3D chips are in great need. This paper discusses the use of a grid and non-uniform placement of TSVs as an effective mechanism for thermal balancing and control in 3D chips. We have modelled the material layers and TSVs mathematically using a detailed calibration phase based on a real 5-tier 3D chip stack, where several heaters and sensors are manufactured to study the heat diffusion. The obtained results show interesting conclusions and new in- sights in the area of thermal modeling and optimization for 3D chips using TSVs.

1 Introduction

Three-dimensional (3D) integration consists of the vertical placement and interconnections of several layers of active circuits. The main interests of this technology are to reduce global interconnect lengths, to increase circuit functionality and to enable new 3D circuit architectures [1, 2, 3].

A key component of 3D technology is a Through-silicon via (TSV) that enables communication between the two dies as well as with the package. Some work has been reported on optimizing the problem of placement of vias for heat dissipation

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in 3D ICs [4, 5]. Other works [6] propose analytical and finite-element models of heat transfer in 3D electronic circuits and use this model to analyze the impact of various geometric parameters and thermophysical properties (through silicon vias, inter-die bonding layers, etc.) on thermal performance of a 3D IC.

This is the first time that a nano-structure of TSVs is proposed on purpose as an effective way to optimize the thermal profile in 3D stacks. The closest work to our proposal is [7], where the authors analyze the impact of thermal through silicon vias (TTVs) in vertically integrated die-stacked devices. However, while the work presented in [7] performs a theoretical analysis, our approach proposes an accurate thermal modeling of the through-silicon vias and it is validated against measurements collected in a real chip. Finally, the thermal effect of the nano-structure of the TSVs will be examined.

The experimental work of this paper is carried out through a novel thermal analysis of a real 5-tier 3D stack (see Figure 1). Then, the material layers and TSVs are modeled mathematically, and the effect of a non-homogeneous distribution of the vias for thermal control is analyzed and effective inclusion of localized TSVs conforming a grid of nano-structures for thermal control is proposed. Also, the effect of specific interface materials used as inter-layer glue is considered. These interfaces will expose unique characteristics due to the presence of aluminium dopants.

The paper structure is as follows: Section 2 presents the configuration of the 3D stack developed for the experimental work, and the developed thermal model is explained in Section 3. Then, the experimental work is covered in Section 4. Finally, the conclusions of the work are drawn.

2 Configuration of the 3D Stack

The 3D chip manufactured for our experimental set-up is created as a multi-level chip, built by stacking silicon layers and fixed with an interface glue. In this configuration, we can find five silicon layers (Die 1 - Die 5), the epoxy-based interface glue, and a bottom PCB layer (see Figure 1). Each stack has an area of 1 cm^2.

This 3D stack resembles the thermal effects that can be found in a 3D multi-processor systems on chip by the use of heaters that create the power dissipation. As the power dissipated in a chip is not uniform on its surface (microprocessors can dissipate between 200 to 300 W/cm^2 while memories only dissipate about $10W/cm^2$) each layer contains several microheaters located at different points to simulate the heat dissipated by the integrated components.

These microheaters are built as a serpentine wire created with thin-film technologies. The material used for the heaters is Platinum, due to its capability to operate at very high temperature and its long stability.

Some thermal sensors are also placed in specific places as detector devices to monitor the temperature inside of the stack and check the heat dissipated and the heat interactions between neighboring microheaters. Platinum has also been selected as the material to build the sensors; therefore, sensors and microheaters

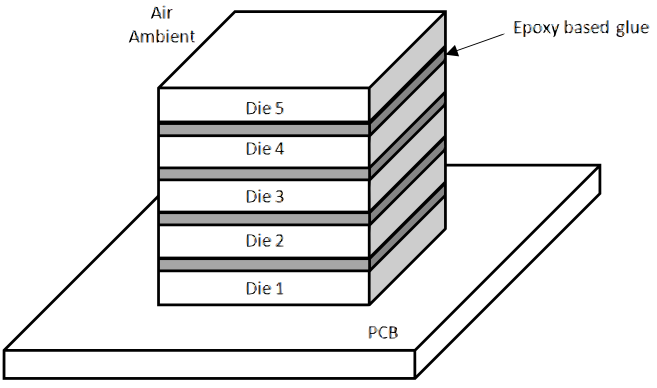


Fig. 1. The test 3D stacked structure

can be manufactured at the same time in a single step of the technology process. These sensors are Resistance Temperature Detectors (RTDs). In this way, the temperature of the heater creates a variation in the resistance of the sensor. Then, the temperature can be obtained by the observation of the voltage drop at both extremities of the sensor (with a fixed current) and applying the resistivity temperature dependence of Platinum.

Each layer comprises 10 heaters of $1mm^2$ each, very similar to the area of common processing elements. These microheaters have been designed to resemble a hot-spot on the surface of the chip of $300W/cm^2$; therefore, each heater dissipates 3 W. The heaters are aligned in three vertical lines. The 5 layers of the stack have the same configuration so the alignment of the heaters appears also out of the plane.

In our configuration, RTDs are placed around the heaters. These sensors are designed for a value of 100 Ω and are driven with a current of 1 mA.

3 Thermal Model

The test five layered 3D stack structure considered in this work is shown in Figure 1. As seen in this figure, five silicon dies, stacked one on the top of another fixed with an interface epoxy glue, are placed on the printed circuit board (PCB). The bottom surface of the 3D stack attached to the PCB is assumed to be adiabatic; therefore, the heat will be exchanged through the vertical active and interface layers in the system.

Within each die, the aluminum resistor-based heaters are fabricated in the silicon dioxide layer on the top of the substrate. These heaters model the thermal effects of the hot-spot cores in an actual 3D MPSoC. The heat generated by these heaters flows through the body of the 3D stack, and ends at the environment interface (ambient) where it is spread through natural convection.

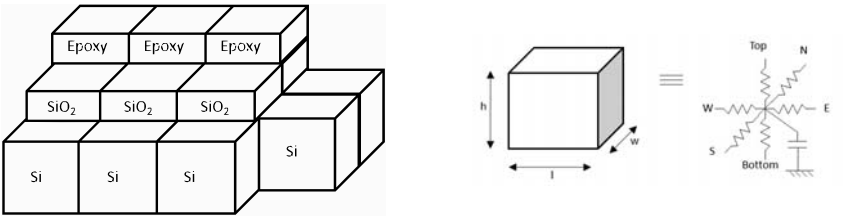


Fig. 2. (a) The unitary thermal cells of the 3D stack (b) Equivalent RC circuit of a single cell

Table 1. Thermal properties of materials

Silicon thermal conductivity	$295 - 0.491T\ W/mK$
Silicon specific heat	$1.659 \times 10^6\ J/m^3K$
SiO_2 thermal conductivity	$1.38\ W/mK$
SiO_2 specific heat	$4.180 \times 10^6\ J/m^3K$
Aluminum electrical resistivity	$2.82 \times 10^{-8}(1 + 0.0039\Delta T)\ \Omega m$ $\Delta T = T - 293.15K$

The heat flow inside this structure is diffusive in nature and hence, is modeled by its equivalence to an electronic RC circuit [8,9,10]. This is done by first dividing the entire structure into small cubical thermal cells as shown in Figure 2a. Each cell is then modeled as a node containing six resistances that represent the conduction of heat in all the six directions (top, bottom, north, south, east and west), and a capacitance that represents the heat storage inside the cell, as shown in Figure 2b.

Current sources, representing the sources of heat, are connected to the cells in the regions where the Aluminum heaters are present. The entire circuit is grounded to the ambient temperature at the top and the side boundaries of the 3D stack through resistances, which represent the thermal resistance from the chip to the air ambient.

The behavior of the resulting RC circuit can be described using a set of first order differential equations via nodal analysis [11].

This model considers the temperature-dependent thermal conductivity of silicon and the temperature-dependent electrical resistance of the aluminum heaters respectively. In this work, a first-order dependence of these parameters on temperatures around 300K is assumed. Some of these parameters are shown in Table 1 [12].

For the validation of the thermal library, profuse temperature measurements on the 3D stack were performed with DC current inputs for the heaters.

4 Electrical Measurements

During the last years, many fabrication-based solutions for the thermal management in 3D integrated circuits have been proposed. Thermal through silicon

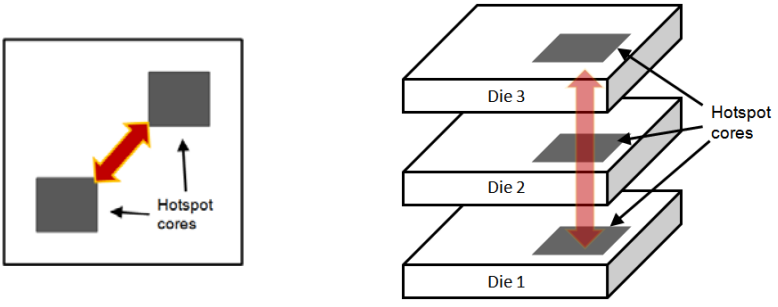


Fig. 3. Communication between active cores in a 3D IC (a)within one layer (b)between different layers

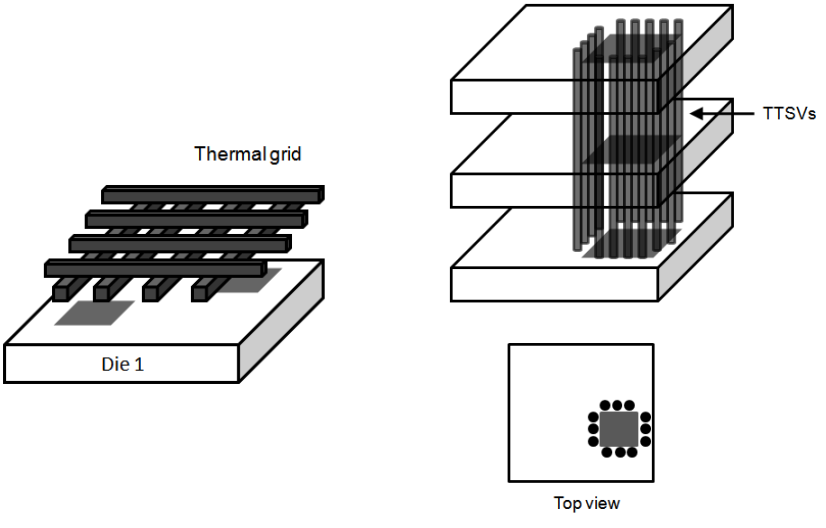


Fig. 4. (a) Thermal grid for reducing temperature variation within a single layer (b) TTSVs for reducing temperature variations along the different layers in a 3D IC

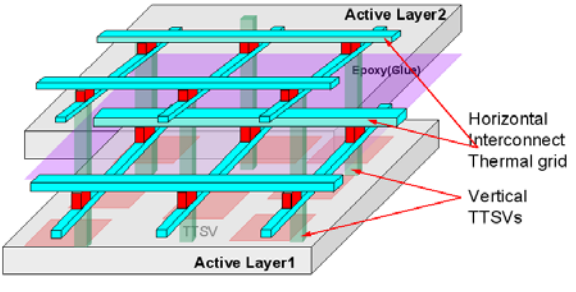


Fig. 5. Vertical and horizontal thermal grid

vias (TTSVs) have a prominent place among these solutions. Many times, it is more desirable to reduce the difference in the temperatures between various parts of the IC, rather than the reduction of the absolute temperature of the chip. This is because variations in operating temperatures affects performance of different parts of the IC (e.g. processor and memory) differently, leading to timing errors and chip failures. Moreover, thermal gradients have been observed as a determinant negative factor on system reliability.

To overcome the above mentioned challenges and to simulate the effects of on-chip metallizations on the thermal behavior of the 3D stack, thermal through silicon vias and thermal grids were introduced in the thermal model developed in the previous section. For the ensuing experiments, a 3-layered 3D stack was used instead of the 5-layered stack. Figure 3 shows two test cases- (a) with 2 hot-spot cores in the same die of the 3D stack and (b) with 3 cores, one on the top of another, communicating each other through different layers (from the performance-enhancement perspective, it is desirable to place the most frequently communicating cores of a 3D IC one on the top of the other to reduce communication delay).

For case (a), to reduce the temperature variations within the same layer, thermal grid networks- dedicated metallizations as well as existing metallizations for the electronic design, are proposed. These thermal grid networks lower the effective thermal conductivity of the dielectric material within the layer and hence, reduce the temperature variations in the layer. This is illustrated in Figure 4a shows the schematic configuration of the horizontal grid.

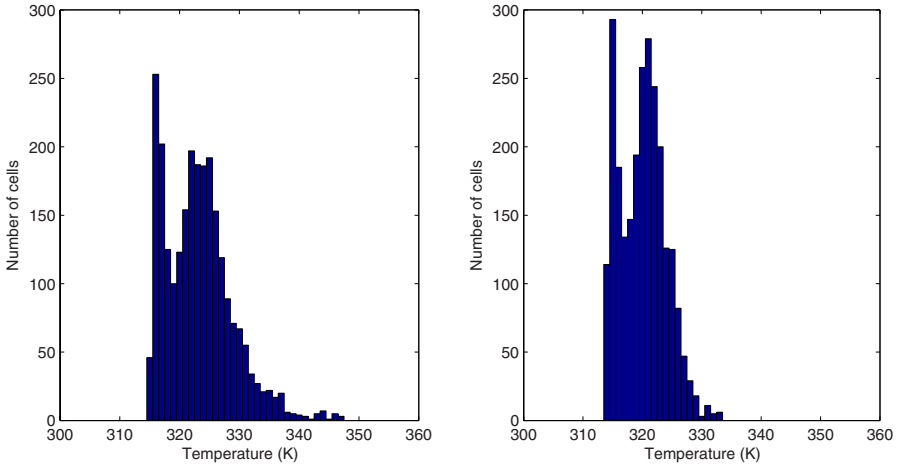
For case (b), to address the temperature variations between different layers in regions where the communicating cores exist, TTSVs are placed around the active cores as shown in Figure 4b. This placement of TTSVs, in addition with the metallizations that naturally exist between the cores meant for electronic routing, reduces the effective thermal conductivity of this region. This, in turn, brings the temperature of different parts of this region closer to each other because of the favored thermal flow.

To incorporate both the thermal grid and the TTSVs in the thermal model, effective thermal conductivity was calculated for the cells in the region containing these metallizations, using the following relation:

$$k_{eff} = k_{cu}\omega + k_{th}(1 - \omega), \tag{1}$$

where, k_{cu} is the thermal conductivity of copper (the metal used for all metallizations in the IC), k_{th} is the thermal conductivity of the surrounding material and ω is the wiring/via density in the region. In the case of TTSVs, a slight modification was made for the effective thermal conductance in the lateral direction. This parameter was calculated by computing the equivalent thermal resistance of the cells depending upon the path of heat flow while traversing it along north-south and east-west direction (a series/parallel combination of vias and surrounding material). Hence, anisotropic cells were created in order to more accurately capture the effects of TTSVs.

Figure 5 shows the devised nano-grid of horizontal interconnects and vertical TTSVs. The TTSVs that integrate the nano-structure improve the overall



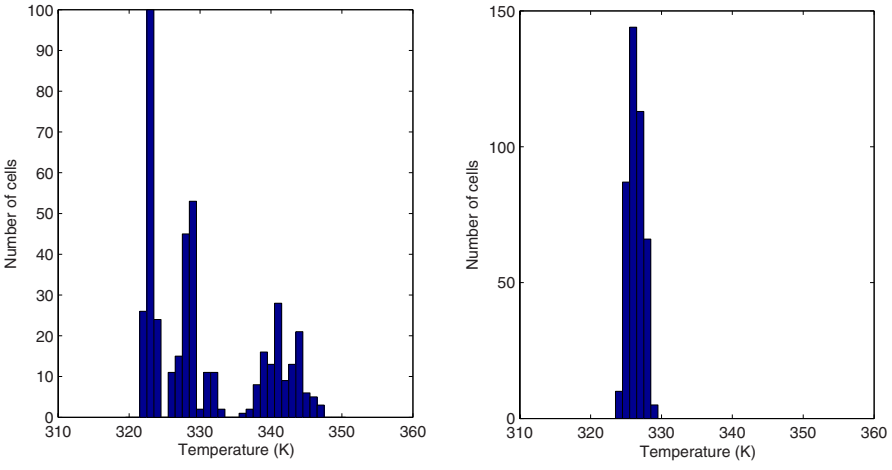
(a) (b)

Fig. 6. Lateral temperature distribution profile for Die 1 (a)without thermal grid and (b)with thermal grid

thermal conductivity of the active layer, provided the thermal coupling is good between the TTSVs. To improve the thermal coupling, these TTSVs must be placed as close as possible to each other but electrically isolated. On the other hand, the horizontal grid helps to spread the temperature along the die and also improve the thermal conductivity of the Inter-Layer Material.

Two experiments were performed to measure the performance of these two strategies. In the first experiment, 4 heaters (in devices D02, D04, D07 and D10) in Die 1 of the 3-layered 3D stack were excited, each with a current of 300 mA ($1.25W/mm^2$). First, this experimental set up was simulated without any thermal grid. Next, thermal grid was added to Die 1 (with 50% wiring density) in the same experimental set up and the resulting model was simulated again. The temperature distribution profile was drawn for each case. These histograms are shown in Figure 6. As can be seen from this figure, the temperature spread within this layer has been reduced by the effect of the thermal grid, that easies the diffusion of the extra heat.

In the next experiment, the same set up was used. TTSVs were laid around each of the active heaters in Die 1. The resulting thermal circuit was then simulated, once without the TTSVs and then once with the TTSVs. Temperatures in the region covered by the TTSVs of one of the heaters (the region enclosed by the TTSVs encompassing all the 3 dies) were recorded in each case. The corresponding temperature distribution profiles for one such active heater regions are shown in Figure 7. We find that the temperature spread was considerably reduced in this region along the vertical direction. Therefore, the grid of TTSVs can be considered as an effective mechanism to optimize the thermal profile in 3D stacks, both in the vertical and lateral direction.



(a) (b)

Fig. 7. Vertical temperature distribution profile for region around D06 (a)without TTSVs and (b)with TTSVs

5 Conclusion

This paper presents a nano-grid of TSVs as an effective mechanism to optimize the thermal profile in 3D integrated systems. In this work, an accurate modeling of the thermal effects that appear in these structures has been developed, and a profuse validation process has been carried out.

The proposed thermal model has then used to evaluate the capability of a nano-structure of thermal through-silicon vias to improve the thermal response of a complex 3D system. The nano-grid is configured to reduce the impact of high-density temperature hot-spots, providing very positive results in the optimization and homogenization of the vertical and lateral diffusion of heat.

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