Optimization of Nanoelectronic Systems Reliability by Reducing Logic Depth

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Abstract. In this paper we address the possibility to improve the reliability of small to middle-size circuits without employing redundancy. Circuits' reliability is improved by reducing the logic depth of critical paths since the probability of failure of each output of the circuit depends no the logic depth of critical paths. Circuits of the same size were considered, as well as different synthesized versions of the same circuit and the estimation of the probability of failure is given with respect to the logic depth.

Keywords: Fault-tolerance, high defect density, logic depth, redundancy, reliability of nanoelectronic systems.

1 Introduction

CMOS scaling has been the trend for decades and even though it has faced many barriers, clever engineering solutions and new device architectures have thus far broken through such barriers enabling scaling to continue at the same speed, and possibly at a slightly slower pace for the next ten years. The nano-age has already begun, where typical feature dimensions are considered to be less than 100 nm. The operation frequency is expected to increase up to 12 GHz, and a single chip will contain over 12 billion transistors in 2020 as given by ITRS [1].

Future systems based on non-CMOS nanoelectronic devices are expected to suffer from low reliability due to both permanent and transient errors. Permanent error rate will increase due to constraints imposed by fabrication technologies. Transient errors rate will increase due to nondeterministic parasitic effects such as background charge, which may disrupt correct operation of single devices both in time and space in a random way. Higher operating frequencies pose strict limits to timing and therefore also introduce the probability of timing errors.

The increased integration of devices on a single die raises the probability of erroneous components in a die, and the individual device failure rates also increase. Conventional fault-tolerant design methods perform efficiently in the context of low failure density encountered so far. The massive nature of defects during manufacturing of nanoscale or molecular scale devices [2,3] expected to plague early generations of nanometric devices demand fundamentally original approaches to

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be applied. Fault-tolerant computing has offered solutions at different abstraction levels of the integration flow to address reliability and fault-tolerance.

Most of the reliability techniques include functional redundancy. Since the improvement of the reliability of redundant units significantly reduces necessary redundancy factors and the overhead [4], exploiting the so-called local level reliability improvement has recently attracted attention of the research community [5,6].

The organization of the paper is as follows. In Section 2 an estimation of the probability of failure of the circuit is given with respect to the logic depth of its critical paths. The probability of failure for the same testbench circuit synthesized for different logic depth of critical paths and the conclusion are presented in Section 3.

2 Dependency of Reliability on Logic Depth

An accurate estimation and evaluation of the local level reliability is crucial for subsequent system level reliability evaluation and optimization. The probability of failure of each output of a unit strongly depends on the logic depth of its critical paths, as demonstrated later in this paper.

The sample circuits used in the following analysis are obtained by partitioning a large design (12-bit look-up table) into various circuits of different logic depths, ranging from two to fifteen. The partitioning is performed using a customized partitioner based on hMetis [7] that has a logic depth minimization goal. A 12-bit look-up table that performs a bijective function, mapping each 12-bit input into one 12-bit output has been chosen as an example design. This choice of design has two important benefits: i) uniform size of subcircuits that are in the output cone of each output – uniform size and connectivity density of networks that belong to longest paths and ii) random internal connectivity. The 12-bit look-up table has been modeled in VHDL and synthesized using Synopsis and subset of Artisan standard library consisting only of inverters and 2 and 3 input NAND and NOR gates. The reduction of the used cell library does not reduce the generality and the analysis could be easily conducted for circuits consisting of any type of gates. The full design consists of approximately 10^5 transistors.

After partitioning this large design using various partition sizes, subcircuits that represent an output cone of each output in every partition are taken as sample circuits and sorted according to the logic depth of critical paths. Therefore, each sample circuit has one output.

The probability of failure of sample circuits is directly acquired using the Monte Carlo (MC) tool described in [8,9]. The tool provides values of the probability of failure of the output of the circuit (probability of circuit failure – P^{unit}_{fails}). The used fault models assume permanent ('hard') faults that are constantly present in the system and the probability of circuit failure is calculated as the worst case of all possible input vectors.

The statistics of the probability of failure for each logic depth is evaluated and the mean value, the 95% confidence interval and the upper bound are derived. More than 100 sample circuits have been evaluated for each logic depth.

The mean values, as well as the bounds of the 95% confidence interval are given in Table 1 in units of the probability of failure of an equivalent gate (P^{gate}_{fails}). It is assumed that the equivalent gate consists of four transistors and that it fails for some fault types. On the other hand, some failures can be masked. Therefore, P^{gate}_{fails} is proportional to the probability of individual device failure (p_f) and to the number of transistor with an empirical coefficient k,

$$P^{gate}_{fails} = 4kp_f \tag{1}$$

where $k = 0.2$ is a typical value for standard library gates (inverters and 2 and 3 input NAND and NOR gates) extracted using MC tool [8,9]. This agrees well with the results presented in [10]. The results for logic depth values up to 15 are presented. For higher logic depths the extrapolation based on the extracted dependency is used, since circuits with logic depths higher than 15 are very large and impractical for statistical evaluation.

Table 1. The probability of circuit failure vs. logic depth (L)

Logic depth L	P^{unit}_{fails}	**95% confidence interval for P^{unit}_{fails}**
2	$2.25 \times P^{gate}_{fails}$	$[1.62,\ 2.88] \times P^{gate}_{fails}$
4	$5.67 \times P^{gate}_{fails}$	$[3.88,\ 7.46] \times P^{gate}_{fails}$
6	$11.63 \times P^{gate}_{fails}$	$[8.03,\ 15.23] \times P^{gate}_{fails}$
8	$20.86 \times P^{gate}_{fails}$	$[14.44,\ 27.28] \times P^{gate}_{fails}$
10	$38.56 \times P^{gate}_{fails}$	$[28.36,\ 48.76] \times P^{gate}_{fails}$
12	$59.32 \times P^{gate}_{fails}$	$[42.01,\ 76.63] \times P^{gate}_{fails}$
15	$117.89 \times P^{gate}_{fails}$	$[79.25,\ 156.53] \times P^{gate}_{fails}$

The dependence of the probability of failure on the logic depth is empirically demonstrated to be exponential and in the form given as

$$P^{unit}_{fails} = \sum_{i=1}^{L} F^{i-1} \cdot P^{gate}_{fails}, \tag{2}$$

where F is a parameter that is extracted through the fitting process, L is the logic depth of the circuit critical paths.

To understand the dependence expressed in (2) the following tree model of the circuit with a single output is presented, illustrated in Figure 1 where a tree structure of a circuit consisting of NAND gates is shown. Each NAND gate in the circuit has F inputs and the probability of failure of each gate is P^{gate}_{fails}. Therefore, F can be understood as the effective fan-in of the gates. For example, if the effective fan-in is two, the total number of gates in the tree is $2^L - 1$ and the whole circuit is assumed to fail if any of the gates fail. Therefore, $P^{unit}_{fails} = (2^L - 1) \cdot P^{gate}_{fails}$. However, in practice the tree structure of the circuit is not complete and has less than $(2^L - 1)$ gates. The upper bound of probability

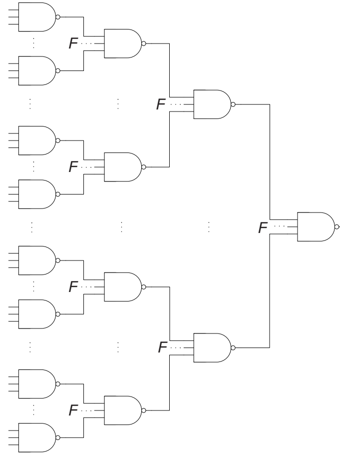

Fig. 1. Tree circuit model with F inputs for each gate

Table 2. The probability of circuit failure vs. logic depth (L) for $L > 15$

Logic depth L	P_{fails}^{unit}
18	$388 \times P_{fails}^{gate}$
20	$1170 \times P_{fails}^{gate}$
25	$5688 \times P_{fails}^{gate}$
30	$31770 \times P_{fails}^{gate}$
35	$182360 \times P_{fails}^{gate}$
40	$1051800 \times P_{fails}^{gate}$

of failure of the circuit is actually given by (2). Hence, we assume that every single output circuit can be represented in the format of this tree structure and through the fitting process we are extracting the effective number of inputs that each gate in the equivalent tree circuit would have.

For each logic depth, the average value of the probability of circuit failure is extracted and the value of F parameter is numerically calculated. The following value is obtained (95% confidence parameter interval in brackets): $F = 1.33\,[1.24, 1.42]$. Since we are targeting the worst case, the upper bound value of 1.42 is taken as the value of the parameter. In Table 2, values of P_{fails}^{unit} are calculated for higher logic depths, using (2) and the upper bound of the fitted F parameter.

3 Reliability Improvement by Logic Depth Reduction

The fact that the probability of failure of a circuit depends on the logic depth of its critical paths can be exploited for redundancy-free local reliability

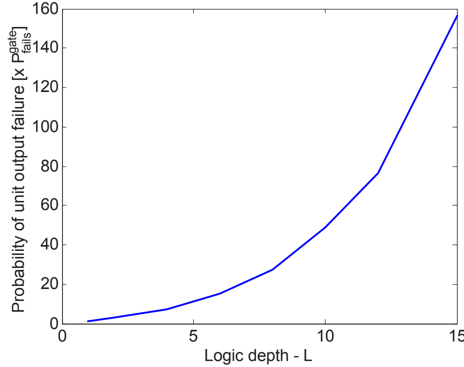

Fig. 2. Upper bound of probability of circuit failure vs. logic depth (L)

optimization. It is called redundancy-free because no redundancy is used in the circuit to achieve improvements in reliability.

In order to perform reliability improvement, a circuit can be synthesized in such a way that the logic depth of its critical paths is the minimal possible, and therefore its probability of failure is also reduced compared to non-optimal logic depth synthesis. To support these claims, an example using LGSynth'91 [11] benchmark circuit *b9* is evaluated with respect to its reliability, considering synthesized versions with different logic depths of critical paths, namely 7, 8, 9 and 10. *b9* is a mid-size benchmark circuit consisting of approximately 400 transistors, 41 inputs and 21 outputs. The probability of failure is evaluated using the MC tool [8,9] for all outputs, and for p_f ranging from 0.001 to 0.01. Detailed MC simulations are used for better accuracy for $p_f = 0.005$. The values of P^{unit}_{fails} for the most unreliable output and an average value over all outputs are reported in Table 3 for all four versions of *b9*.

Table 3. Probability of failure of the *b9* benchmark output vs. logic depth of the synthesized version for $p_f = 0.005$

Logic depth	**Size**	P^{unit}_{fails} **per output**	
L	**[num. eq. trans.]**	**most unreliable**	**average**
7	424	0.134	0.065
8	384	0.135	0.069
9	354	0.115	0.072
10	388	0.121	0.079

The improvement in reliability between the versions with $L = 10$ and $L = 7$ equals 21.5% when the probability of failure is averaged over all outputs for $p_f = 0.005$. A constant improvement in reliability is noticeable with the reduction of the logic depth for all device probabilities of failure. For individual outputs,

this is not necessarily the case, because the logic depth of the given output cone changes between different realizations. The average improvement in reliability for all device probabilities of failure averaged over all outputs is 18.8%. Realizations of the circuit with smaller logic depth have, in general, bigger sizes in terms of the number of equivalent transistors. The difference equals 16.5% between the smallest and the largest version.

In this paper an estimation of the probability of failure of small to mid-sized circuits has been given with respect to the logic depth of these circuits. The constant improvement in reliability has been demonstrated on same circuit synthesized for shorter critical paths. This enables efficient local optimization by circuit resynthesis, having the logic depth as the minimization goal.

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