FPAA Based on Integration of CMOS and Nanojunction Devices for Neuromorphic Applications

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Abstract. In this paper, a novel field programmable analog arrays (FPAA) architecture, namely, NueroFPAA, is introduced to utilize nanodevices to build a programmable neuromorphic system. By using nanodevices as programmable components, the proposed FPAA can achieve high-density and low-power operations for neuromorphic applications. The routing and function blocks of the FPAA are specifically designed so that this proposed architecture can support large-scale neuromorphic design as well as various analog circuitries.

Keywords: Field programmable analog arrays (FPAA), Nanojunction devices, Operational amplifier (Op-amp).

1 Introduction

Field-programmable analogue array (FPAA) is a reconfigurable platform to build analog circuits and can dramatically reduce time-to-market in analog circuit development [1-4]. One promising application of FPAA is to build a neuromorphic system that can mimic human brain. Such intelligent computing systems can carry out analog computation with extremely low power consumption, which can outperform the traditional digital computers for various applications such as pattern recognition and classification [4-8]. Even though FPAA is an efficient reconfigurable platform to establish electronic neuromorphic machine, the device density and complexity of the current FPAA needs to be significantly increased. The typical neuromorphic system scalable to biological levels will require a density of 1010 nodes/cm2 and a complexity of 1014 components. In order to achieve such a high density and large complexity, new devices and architectures of FPAA need to be developed.

In this paper, we introduce a new FPAA structure, namely, nueroFPAA, by utilizing CMOS devices as logics and emerging memory devices as programming elements. In particular, we use resistive junction to build the programmable elements in both routing channel and function block of a FPAA. The nanojunction device is a metal-insulator-metal nanojunction with hysteretic resistance characteristics. The routing channel based on these junctions can work as the synapses reaching a density of 1010/cm2 [5-8]. The function block based on a combination of CMOS and junction devices will be a reconfigurable component as neurons. Therefore, the proposed

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system not only can support the complex analog applications such as filters, differentiators, but also can provide an efficient platform to build neuromorphic system that mimic human brain.

2 Proposed Neuro-FPAA Architecture

In this section, we will first review the existing FPAA structure [1] and then develop a new neuroFPAA architecture to utilize the nanojunction devices with CMOS devices for neuromorphic applications.

2.1 FPAA Basics

FPAA mainly consists of: (1) routing channel that connects the function blocks. (2) Functional blocks or configurable analog blocks that implement circuit functions. Both routing channel and function block have the reconfigurable capabilities.

The routing channel is based on the global and local crossbars. At each crosspoint of the crossbar, a floating gate is required to provide reconfigurable capabilities. The CAB consists of Op-amp, detector, SOS, matrix multiplier, peak detector and capacitors. The configurable capabilities of CAB come from the local crossbar that connects the CAB.

This existing FPAA architecture is sufficient for analog circuit development. However, for the neuromorphic application, the size of the crossbar is increasing. The size of crossbar will be considerably large due to the use of floating gate transistors. This motivates us to use nanojunction to replace floating gate to achieve a high-density FPAA.

2.2 Proposed Neuro-FPAA

As shown in Fig. 1, the proposed FPAA architecture contains routing crossbars based on nanojunctions and CABs incorporating nanojunctions inside to obtain CAB programmable capabilities. The arrangement of routing and CAB in Fig. 1 is specifically suitable for neuromorphic applications.

Nanojunction-Based Routing for Synaptic Operations: Fig. 1 shows the feed forward case such that each CAB will reach two following CABs through the routing crossbar. Each CAB consists of 10 neurons and the size of the routing crossbar is 38*19.

By utilizing the crossnet concept, the neural network applications will require the presynaptic neuron to reach the postsynaptic neuron using two different paths. For example, the same output signals of a neuron in CAB-I will reach a neuron of CAB-II in two paths. Using two other paths, CAB-I will also reach CAB-III. Therefore, each neuron can reach 20 neurons, requiring 38 paths.

If the recurrent neural network is implemented, each forward path will have a corresponding backward path that is in parallel to the forward path with a reverse direction. Thus, the crossbar will be duplicated for this purpose.

Nanojunction-Based CAB as Neuron: The CAB consists of 10 neurons. Each neuron is essentially an Op-amp with R, C supporting elements. The Op-amp and its internal

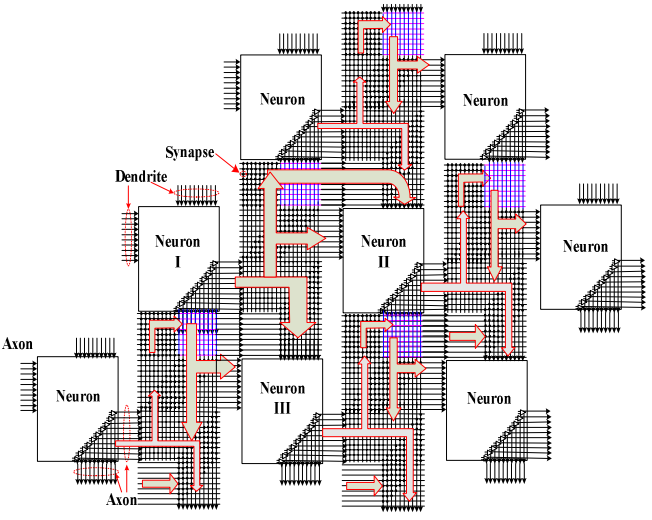

Fig. 1. Proposed neuroFPAA architecture

arrangement strongly affect the flexibility and functionality of the neuron. Thus, we propose a CAB with 10 Op-amps and several programmable capacitor arrays (PCAs), programmable resistor arrays (PRAs). The nanojunctions are also included in the PRAs and PCAs to provide programmable capabilities (see Fig. 1).

Note that the PCA and PRA are not only useful the neuron application but also can realize feedback loop, signal coupling, integration, differentiation and other analog signal processing functions. In this way, this proposed CAB structure can fulfill the requirement of general FPAA analog circuit applications as well as neuromorphic applications.

Improved Op-amp in CAB: The Op-amp is the core building block for a neuroFPAA. It should have adaptability and flexibility. In our design, applications of operational amplifiers include non-linear circuit's application and linear circuit's application. Non-linear applications include: neuron, logarithmic amplifier, and exponential amplifier. Linear applications include: voltage to current converters, current to voltage converters, summing amplifier inverter, noninverter, the integrator, and the differentiator.

We specifically improve the Op-amp design to achieve high performance both types of applications. It is a two-stage design consisting of a folded-cascade amplifier, source follower and compensation network. By using this improved design, the properties of Op-amp in terms of gain and phase margin, power supply rejection ratio and common-mode rejection ratio are significantly improved.

3 Operation Analysis and Performance Evaluation

The operation of the proposed FPAA as a neural network consists of two steps: training and operation. To statically train the routing crossbar, the dedicated programming

circuitry (not shown in Fig. 1) is required to configure the synaptic junction a prior. This is generally referred to pre-computation training. The second method is called "in situ" training. Since the junction is a two terminal device, we can also modulate the current and voltage of neuron to program the junction dynamically.

After the training or configuration step is over, the neuroFPAA is changed to operation mode. The input signals are inserted into the network and allow the synapses and neurons to start operations.

During the operation, the system can have defect tolerance and low-power performance. The junction devices may have high defect rates. The nanowire connections can also be defective. However, since NN can function with these defective devices while maintaining minimal performance degradation, the neuromorphic system can provide high defect tolerance: in some cases, it can provide 99% fidelity with more than 80% fraction of bad devices [8].

The low-power properties of the system stem from the low working frequency. The system is generally working in 100HZ and KHz ranges [9], leading to low power consumption.

3.1 Performance Evaluation

The performance analysis is carried out based on the estimation of nanojunction performance, which will be compared with floating gate devices. The 38*19 crossbar will require 722 transistors (T) in the floating gate based FPAA structure. By using the nanojunctions, we can expect to reduce the size by 10 times (assuming the 10 junctions will be equivalent to 1 transistor) [11].

The operational speed of the proposed neuroFPAA and the floating gate transistor-based FPAA can be the same. Since the proposed structure reduces the area of the crossbar by 10X and the crossbar will be half of the complete FPAA (the CAB area is not reduced), the power consumption of the whole system is expected to be reduced by 5X.

4 Conclusion

The significance of this work is that this study introduces an efficient reconfigurable platform for large scale neuromorphic system designs by utilizing nanodevices with CMOS devices. By utilizing nanojunction devices, the proposed nueroFPAA can achieve high-density and low-power operations. The proposed routing and function blocks are specifically designed to suit for both large-scale neuromorphic applications and general analog circuit designs.

A preliminary comparison study is also carried out to compare the existing floating gate-based FPAA and the proposed neuroFPAA. The results demonstrate that by replacing floating gate devices with nanojunction, the density and power can be significantly reduced. However the reproducibility and stability of the nanojunction devices are worse than those of the floating gate transistors. Significant progress is expected to advance the fabrication of nanojunction to enable the proposed neuroFPAA into reality.

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