Normal and Reverse Temperature Dependence in Variation-Tolerant Nanoscale Systems with High-k Dielectrics and Metal Gates

David Wolpert and Paul Ampadu

Electrical and Computer Engineering Department
University of Rochester, Rochester, NY 14627, USA
{wolpert,ampadu}@ece.rochester.edu

Abstract. The delay dependence on temperature reverses at increasingly larger supply voltages as technology scales into the nanometer regime, causing delay to decrease as temperature increases. This reversal can be problematic for variation-tolerant systems using critical path replicas to determine delay guardbands, as delay may no longer indicate when the system is in danger of thermal runaway. Adaptive voltage scaling, commonly used in variation-tolerant systems, further complicates the temperature impact, as the range of voltages may intersect both temperature regions. In this paper, it is shown that use of high-k dielectrics and metal gates increases the supply voltage where this reversal occurs by 40% compared to low-k, poly gate technologies. 45, 32, and 22 nm models are examined, and the reversal voltage is shown to approach 90% of nominal voltage at 22 nm, making the effect important even for non-adaptive designs. Techniques to account for these complex temperature dependencies are proposed to ensure functionality under all conditions.

Keywords: Reverse temperature dependence, variation-tolerant, high-k dielectric, metal gate.

1 Introduction

Operating temperature affects device delay by altering mobility (μ) and threshold voltage (V_T), according to [1]

$$\mu\left(T\right) = \mu_0 \left(T/T_0\right)^{\alpha_\mu} \tag{1}$$

and

$$V_T\left(T\right) = V_{T0} + \alpha_{V_T}\left(T - T_0\right). \tag{2}$$

where T_0 is the nominal temperature (generally 300 K), μ_0 is mobility at T_0, α_μ is an empirical parameter referred to as the mobility temperature exponent, V_{T0} is nominal threshold voltage, and $\alpha_{V_T} = \partial V_T/\partial T$ is another empirical parameter named the threshold voltage temperature coefficient.

M. Cheng (Ed.): NanoNet 2008, LNICST 3, pp. 14–18, 2009.

V_T, μ, and nominal supply voltage (V_{DD}) are all technology dependent parameters, with predicted values available down to the 22 nm node [2,3]. Use of high-k dielectrics and metal gates to alleviate nanoscale gate leakage problems also alters V_T and μ [4,5]. The combination of these changes makes it difficult to determine the effect of temperature on device performance. Two temperature regions exist: normal temperature dependence, where current decreases as temperature increases, and reverse temperature dependence [6,7], where current increases as temperature increases.

These parameters are further complicated by environmental requirements (military specifications call for a range of -55°C to 125°C) and intra-die temperature variation (shown to exceed 25°C [8]). To account for the wide range of conditions, as well as process and voltage variations, variation-tolerant adaptive systems have been used to guarantee functionality by adjusting operating voltages and frequencies [9,10,11]; however, these systems with multiple voltage modes make the above-mentioned temperature effects even more difficult to determine.

The remainder of this paper will be organized as follows: In Section 2, the impact of high-k dielectrics and metal gates on temperature behavior will be examined, and the changing impact of temperature across 45, 32, and 22 nm technologies will be shown. In Section 3, the effects of these complex temperature dependencies on variation-tolerant systems are explained, and techniques for considering these dependencies are discussed. Conclusions are presented in Section 4.

2 Temperature Impact on Current and Delay

For large gate overdrives ($V_{GS} - V_T > V_{ti}$, where V_{ti} is an empirical parameter referred to as the temperature insensitive voltage [7]), the temperature dependence of a device is dominated by the dependence of μ, while for small gate overdrives ($V_{GS} - V_T < V_{ti}$), small changes in V_T can cause large changes in current, resulting in a temperature dependence dominated by V_T. The normal temperature dependence occurs when the μ dependence dominates, while the reverse temperature dependence occurs when the V_T dependence dominates. Further examination of these effects in low-k dielectric, polysilicon gate devices is available in [6,7].

In nanoscale devices, high-k dielectrics and metal gates have been introduced to reduce gate leakage due to thinning gate oxides and reduce the depletion effects of polysilicon gates [4,5]; unfortunately, these techniques have the effect of dramatically increasing the temperature dependence on V_T. The extent of this effect is shown in Fig. 1, which compares 45 nm predictive technology models [2] of both low-k/poly gate (dashed line) and high-k/metal gate (solid line) devices. Each line in Fig. 1 shows the change in delay of an inverter ($\beta = 2$) from -55°C to 125°C. For example, at 0.62 V, the high-k/metal gate inverter delay does not change at all from -55°C to 125°C, resulting in the 0.62 V point occurring on the 0% line. This 0% intersect on each curve represents V_{ti}. As shown, the high-k/metal gate devices result in a 40% increase in V_{ti} compared to the low-k, polysilicon gate devices. The normal temperature dependence region is below the 0% line, and the reverse dependence region is above the 0% line.

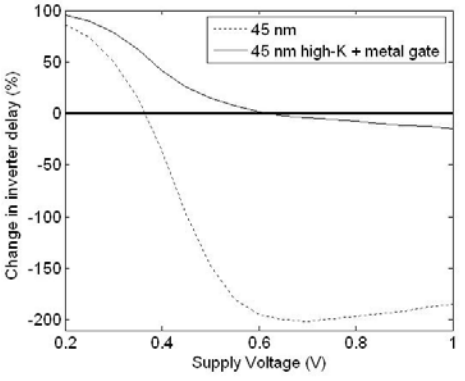

Fig. 1. Effect of high-k dielectric and metal gate on temperature dependence

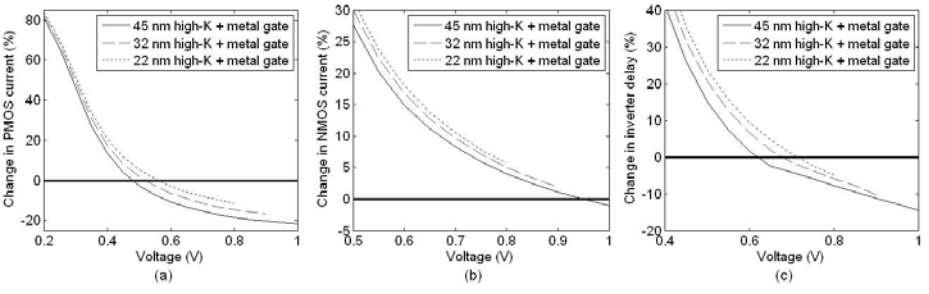

Fig. 2. Changes in (a) PMOS current, (b) NMOS current, and (c) inverter delay over the -55°C to 125°C temperature range

Fig. 2(a) shows the change in PMOS device current from -55°C to 125°C at the 45, 32, and 22 nm technology nodes. Nominal voltage at each node is indicated by the rightmost point on each curve, equal to 1 V, 0.9 V, and 0.8 V, at 45, 32, and 22 nm, respectively [2,3]. As shown, V_{ti} of the PMOS devices steadily increases as technology scales down by about 400 mV (20%) per node, with V_{ti} at 22 nm equal to 0.56 V. The NMOS device response, shown in Fig. 2(b), is quite different, with nominal voltages at the 32 and 22 nm nodes already in the reverse temperature dependence region. The PMOS and NMOS devices are combined into an inverter in Fig. 2(c), with $\beta = 2$ to represent FO4 minimum delay sizing. As shown, V_{ti} in the inverter approaches 90% of nominal voltage in the 22 nm node. As β increases, the stronger PMOS effect further increases V_{ti}. Thus, these complex temperature effects will require attention in nanoscale systems even at nominal voltages.

3 Variation-Tolerant Systems with Complex Temperature Dependences

Reverse temperature dependence at near nominal voltages complicates variation-tolerant system design, which uses multiple supply voltages to adjust for changes

in process, voltage, and temperature. The additional complexity needed to account for both normal and reverse temperature dependence depends on the design time information. If the system can be fully characterized at design time, then this can be solved by updating the voltage and frequency look-up table entries [10] to ensure that the system adapts in the correct direction given a change in temperature. For example, whereas a low-voltage system would generally reduce the frequency as temperature increases, in the reverse dependence region the system would have to reduce the frequency when temperature decreases.

If the temperature regions in some voltage modes are not known at design time, whether due to tool limitations, process variations, or unknown IR drops, they must be determined at runtime. If the system is known to be in the normal temperature dependence region at nominal voltage, then a fixed nominal-voltage ring oscillator can be compared to the critical path replica (whose supply voltage changes with the rest of the system to track the delay at each voltage mode). By comparing the critical path replica delay with the ring oscillator frequency at two different temperatures, the temperature region of each voltage mode can be determined at manufacture time and stored. To include aging effects, this test can be performed at runtime as needed.

If the temperature dependence is not known for every voltage mode, then there are two options for ensuring variation-tolerance. One option is to design the system with large enough guardbands that it can operate correctly over the entire temperature range regardless of the dependence, though this will result in a large reduction in delay performance. Another option is to use a temperature sensor with a poly resistor, which would consume large area and power but avoid the nonlinear effects of mobility and threshold voltage, resulting in a stable reference exhibiting normal temperature dependence regardless of variations.

An important issue with all of the approaches mentioned in this section is that high temperatures in the reverse dependence region are no longer self-limiting: In the normal dependence region, temperatures are unable to increase to dangerous levels because the delay would become so large that the system would be forced to throttle the frequency, reducing the energy and therefore the temperature. In the reverse dependence region, the circuits will continue to speed up as temperature increases, with no such delay problem. This could potentially result in race conditions, or even more concerning, the higher temperatures could result in thermal runaway due to the exponential temperature dependence of leakage current [12], which will already be dominating the total power consumption in the nanoscale regime [13].

4 Conclusion

While the complexities of temperature dependence were previously only an issue in ultra-low voltage design, the combination of high-k dielectrics, metal gates, and nanoscale parameters mean they will require attention even in nominal voltage systems. The reversal of temperature dependence occurs at 90% of the nominal supply voltage at 22 nm, and potentially even higher voltages depending

on device ratios. After considering voltage and process variation effects, unknown temperature dependences may affect any system, whether or not it uses adaptive voltage controls. Techniques for avoiding delay failure and thermal runaway as a result of these complex dependencies will become more and more important as technologies stretch further into the nanoscale regime.

References

1. Filanovsky, I.M., Allam, A.: Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits. IEEE Trans. Circuits and Systems I: Fundamental Theory and Applications 48, 876–884 (2001)
2. Zhao, W., Cao, Y.: New generation of Predictive Technology Model for sub-45nm early design exploration. IEEE Trans. on Electron Devices 53, 2816–2823 (2006)
3. Zhao, W.: Personal communication (2008)
4. Guillaumot, B., et al.: 75nm damascene metal gate and high-k integration for advanced CMOS devices. In: International Electron Devices Meeting, pp. 355–358 (2002)
5. Cheng, B., et al.: The impact of high-k gate dielectrics and metal gate electrodes on sub-100 nm MOSFET's. IEEE Trans. Electron Devices 46, 1537–1544 (1999)
6. Park, C., et al.: Reversal of temperature dependence of integrated circuits operating at very low voltages. In: International Electron Devices Meeting, pp. 71–74 (1995)
7. Bellaouar, A., Fridi, A., Elmasry, M.I., Itoh, K.: Supply voltage scaling for temperature-insensitive CMOS circuit operation. IEEE Trans. Circuits and Systems II: Analog and Digital Signal Processing 45, 415–417 (1998)
8. Sato, T., Ichimiya, J., Ono, N., Hachiya, K., Hashimoto, M.: On-chip thermal gradient analysis and temperature attening for SoC design. IEICE Trans. Fundamentals E88-A, 3382–3389 (2005)
9. Martin, S., Flautner, K., Mudge, T., Blaauw, D.: Combined dynamic voltage scaling and adaptive body biasing for lower power microprocessors under dynamic workloads. In: IEEE/ACM Int. Conf. on Computer Aided Design, pp. 721–725 (2002)
10. Tschanz, J., et al.: Adaptive frequency and biasing techniques for tolerance to dynamic temperature-voltage variations and aging. In: IEEE Int. Solid-State Circuits Conf., pp. 292–293 (2007)
11. Elgebaly, M., Sachdev, M.: Variation-Aware Adaptive Voltage Scaling System. IEEE Trans. Very Large Scale Integration (VLSI) Systems 15, 560–571 (2007)
12. Lee, C.-C., de Groot, J.: On the thermal stability margins of high-leakage current packaged devices. In: 8th Electronics Packaging Technology Conference, pp. 487–491 (2006)
13. Kim, N.S., et al.: Leakage current: Moore's law meets static power. IEEE Computer 36, 68–75 (2003)