A Voltage Controlled Nano Addressing Circuit

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Abstract. A voltage controlled nano addressing circuit is proposed, which (1) improves yield and enables aggressive scaling with no requirement of precise layout design, (2) achieves precision of addressing by transistor current-to-voltage sensitivity in the circuit and applied external address voltages, and (3) is adaptive to and more robust in the presence of process variations which are expected to be prevalent in nanoelectronic designs.

Keywords: Nanoelectronics, Nano Architecture, Nano Addressing.

An outstanding challenge for realizing nanoelectronic systems is how to precisely address a nanoscale wire in an array for configuration or data IO. The existing nano addressing mechanisms are based on binary decoders to select one of 2^n nanoscale data lines based on n microscale address lines. They are either (1) randomized contact decoders [9], (2) addressing undifferentiated nanoscale wires by (lithography defined) differential microscale wires [4], or (3) addressing differentiated nanoscale wires by undifferentiated microscale wires [1,5]. All these existing nano addressing mechanisms require precise layout design, which is unlikely in nanotechnology, wherein regular structures are expected to grow in bottom-up self-assembly processes [6].

I propose a voltage controlled nano addressing circuit (Fig. 1 (left)), which includes two rows of field effect transistors, of which the source/drain regions are connected to the data lines (nanoscale wires, e.g., carbon nanotubes), while the gates are connected to the address lines (which can be microscale wires or even nanoscale wires). Continuously tunable external voltages (V_{dda1}, V_{ssa1}, V_{dda2}, and V_{ssa2}) are applied to the address lines and the transistor gates. All components in this structure are designed as uniform, e.g., the transistors are identical, and the address lines have uniform serial resistance. The external voltages are applied such that a decreasing and an increasing array of gate voltages are applied to the transistors in the first and the second row, respectively. As a result, the data lines have different conductivity depending on their locations. By applying different addressing voltages (V_{dda1}, V_{ssa1}, V_{dda2}, and V_{ssa2}), this circuit is able to selectively address one of the data lines in the array.

For example, to address a carbon nanotube (CNT) in an array, each nanotube is gated by two N-type CNT field effect transistors (CNFETs) [8] of $6.4nm$ gate width and $32nm$ channel length, as are given by the Stanford CNFET

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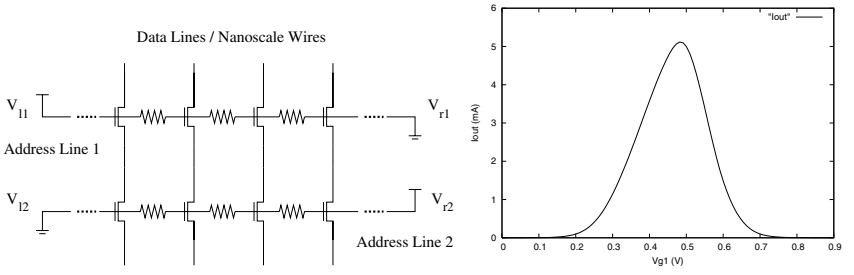

Fig. 1. A voltage controlled nano addressing circuit (left), and nanotube current I_{out} (mA) vs. CNFET gate voltage $V_{g1}(V)$ in the first address line (right)

compact model [2]. The two CNFETs in each nanotube are given a voltage drop of $V_{dd} = 1V$. The external address voltages are $V_{dda1} = V_{dda2} = 1V$, $V_{ssa1} = V_{ssa2} = 0$. SPICE simulation gives the current for each nanotube in the array (data lines) with different gate voltage in the first address line (Fig. 1 (right)). We have the following observations.

1. The nanotubes carry a significant current only with specific gate voltages, allowing addressing of a specific carbon nanotube by applying different addressing voltages.
2. To precisely address a single nanotube, two adjacent nanotubes must carry significant different currents. This can be achieved by (1) increasing the current-to-voltage sensitivity of the transistors [8], or (2) increasing the gate voltage difference between two adjacent nanotubes.
3. Process variations (e.g., of data line shifting and contact resistance) can be cancelled by tuning the addressing voltages, or (e.g., of address line geometry or resistance) have little effect.
4. The proposed circuit requires only uniform components in a regular structure, avoiding precise layout design, which significnatly improves yield and enables aggressive scaling of nanoelectronic systems.

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