Digital Microfluidic Logic Gates

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Abstract. Microfluidic computing is an emerging application for microfluidics technology. We propose microfluidic logic gates based on digital microfluidics. Using the principle of electrowetting-on-dielectric, AND, OR, NOT and XOR gates are implemented through basic droplet-handling operations such as transporting, merging and splitting. The same input-output interpretation enables the cascading of gates to create nontrivial computing systems. We present a potential application for microfluidic logic gates by implementing microfluidic logic operations for on-chip HIV test.

Keywords: microfluidic computing, digital microfluidics, logic gate.

1 Introduction

Microfluidics technology has made great strides in recent years [1]. The applications of this emerging technology include immunoassays, environmental toxicity monitoring and high through-put DNA sequencing. An especially promising technology platform is based on the principle of electrowetting-on-dielectric. Discrete droplets of nanoliter volumes can be manipulated in a "digital" manner on a two-dimensional electrode array. Hence this technology is referred to as "digital microfluidics" [2].

An especially promising application is the use of droplets for microfluidic computing. Microfluidic computing inherits the advantages of both microfluidics for sensing and computing for information processing [3]. The speed of microfluidic computing is much less than silicon-based computing devices. Hence microfluidic computing will not replace conventional computing devices; nevertheless, it will enhance microfluidic technology through direct incorporation of computing functions on-chip with other primary sensing functions. Microfluidic computing devices can be implemented in various ways, such as electrochemical reactions [4], relative resistance [5], bubbles in electronic channels [6]. However, a drawback of these methods is that they assign different interpretations to inputs and outputs, which makes cascading of gates difficult.

We propose logic gates based on digital microfluidics. We implement AND, OR, NOT and XOR gates through basic droplet-handling operations such as transportation, merging, and splitting by using the principle of electrowetting-on-dielectric. Nontrivial computing systems can be created by cascading the microfluidic logic gates that have the same input-output interpretation. A potential

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application for microfluidic logic gates is presented by implementing microfluidic logic operations for on-chip HIV test.

2 Digital Microfluidic Platform

In digital microfluidics, droplets of nanoliter volumes are manipulated on a two-dimensional electrode array [1]. A unit cell in the array includes a pair of electrodes that acts as two parallel plates. The bottom plate contains a patterned array of individually controlled electrodes, and the top plate is coated with a continuous ground electrode. All electrodes are formed by optically transparent indium tin oxide (ITO). A dielectric insulator, i.e., parylene C, coated with a hydrophobic film of Teflon AF, is added to the top and bottom plates to decrease the wettability of the surface and to add capacitance between the droplet and the control electrode. A droplet rests on a hydrophobic surface over an electrode.

Droplets are moved by applying a control voltage to a unit cell adjacent to the droplet and, at the same time, deactivating the cell just under the droplet. This electronic method of wettability control creates interfacial tension gradients that move the droplets to the charged electrode. Fluid-handling operations such as droplet merging, splitting, mixing, and dispensing can be executed in a similar manner. Droplet routes and operation schedules are programmed into a microcontroller that drives the electrodes. Design automation techniques for digital microfluidics are now being developed [10].

3 Digital Microfluidic Logic Gates

In the digital microfluidic platform, droplets of unit volume (1x) or larger can be easily moved [7]. A droplet of 0.5x volume is not large enough to have sufficient overlap with an adjacent electrode; hence it cannot be moved [7]. It has been verified experimentally that the times required for dispensing one droplet, splitting a droplet into two, merging two droplets into one, and transporting a droplet to an adjacent electrode are nearly identical. This duration is defined as one clock cycle.

The definitions for logic values '0' or '1' are as follows: the presence of a droplet of 1x volume at an input or output port indicates a logic value of '1'. The absence of a droplet at an input or output port indicates the logic value '0'. The same interpretations at inputs and outputs enable the output of one gate to be fed as an input to another gate, thus logic gates can be easily cascaded.

Fig. 1 shows the schematics of the 2-input OR, 2-input AND, NOT, and XOR gates. The OR gate in Fig. 1(a) incorporates a waste reservoir (WR) and twelve indexed electrodes. Electrode 1 and Electrode 2 are the two input ports X_1 and X_2; Electrode 3 is the reference port (R), from which one reference droplet is injected into the OR gate. Electrode 9 is the output port (Z) where a detector can be placed to determine the output logic value of the OR gate. Such detections to indicate the presence or absence of a droplet can be easily implemented using capacitive measurements [11]. Electrode 12 is the washing

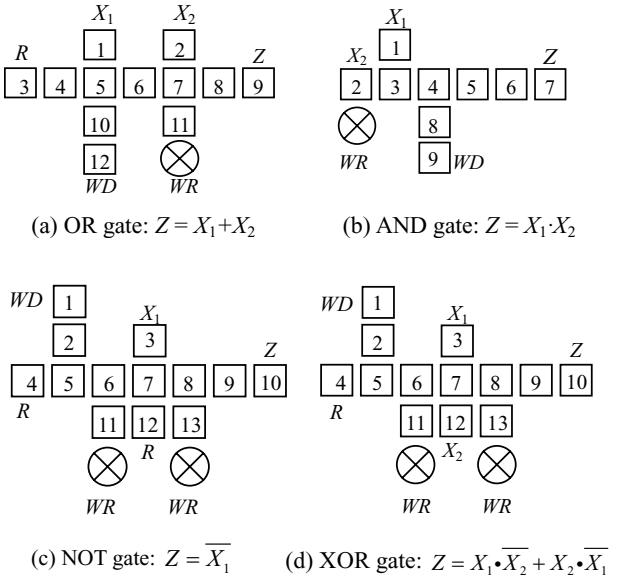

Fig. 1. Schematics of microfluidic logic gates

Table 1. Actuation-voltage sequence for the OR gate

Clock cycle	Electrode No.											
	1	2	3	4	5	6	7	8	9	10	11	12
0	1	1	1	0	0	F	0	F	F	0	F	1
1	0	0	1	0	1	0	1	0	F	0	0	1
2	0	0	1	0	0	1	0	0	F	0	0	1
3	0	0	1	0	1	0	1	0	F	0	0	1
4	0	0	0	1	0	0	0	0	F	0	1	1
5	0	F	0	0	1	0	0	F	F	0	0	1
6	0	F	F	0	0	1	0	F	F	0	F	1
7	F	0	F	F	0	0	1	0	F	0	0	1
8	F	0	F	F	0	1	0	1	0	0	0	1
9	F	F	F	F	0	1	0	0	1	0	F	1

port (WD), from which a washing droplet is injected after the logic operation to collect the residual droplets and move them to the waste reservoir. The sequence of control voltage applied to each electrode is shown in Table 1. A '1' ('0') entry in the table indicates a high (low) voltage to the corresponding electrode in that clock cycle. An 'F' entry indicates a floating signal, i.e., it is not required to be either active or inactive. The sequence of control voltages is independent of the input logic values. Fig. 2 describes the cycle-by-cycle operation of the OR gate for $X_1X_2 = 11$.

The delay of the OR gate is 9 clock cycles, independent of the inputs. At the beginning of clock cycle 10, the droplet on the washing port (Electrode 12) is

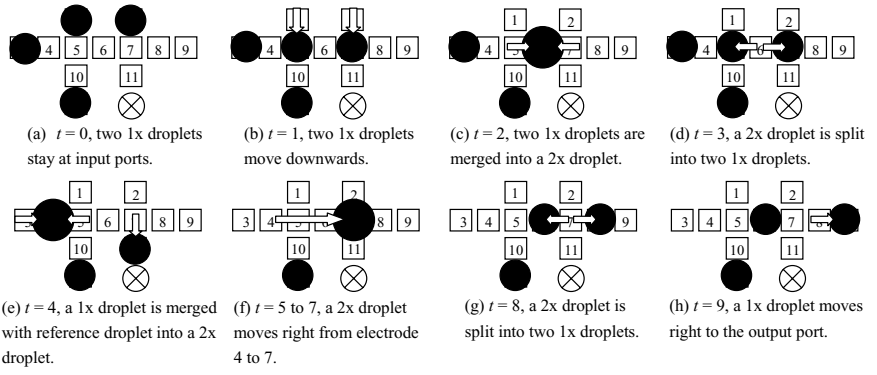

Fig. 2. Operation of the OR gate for input 11

routed to merge with the residual droplets, and the result is transported to the waste reservoir. After this washing process, no droplet is left on the electrodes, and this gate is clean for the next operation.

To experimentally verify the OR gate, we configured it on a fabricated lab-on-chip, then activated the corresponding electrodes to perform on-chip cycle-by-cycle operations in the laboratory. In this experiment, we use a lab-on-chip with an electrode pitch of 1.5 mm and a gap spacing of 0.475 mm. The droplets are dispensed from the on-chip reservoirs that are filled by DI water with black dye. The voltage set-up for the splitting process is 250 V (input voltage for PCB). Under this voltage set-up, the droplet with volume equal to or larger than 1x can be split into two droplets with equal volumes. The voltage set-up for transportation is in the range of 80 V to 90 V (input voltage for PCB). Under this voltage set-up, only droplets with volume equal to or larger than 1x can be

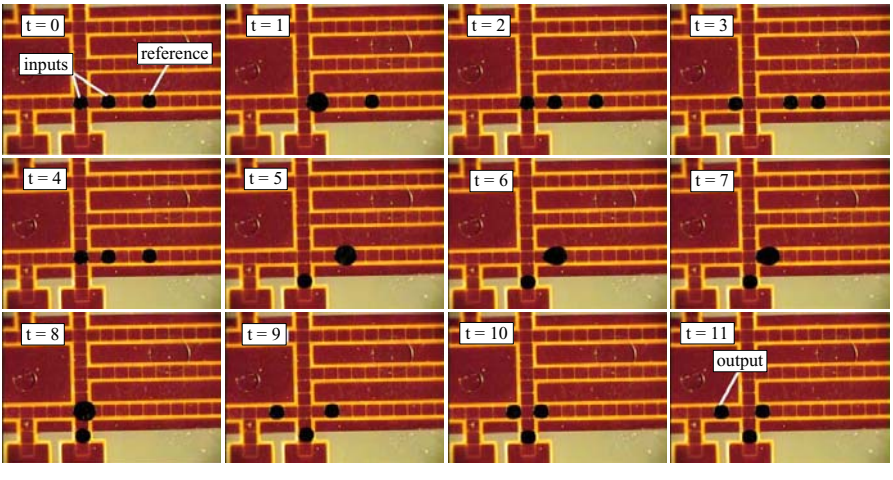

Fig. 3. On-chip cycle-by-cycle operation for the OR gate with input 11

moved to the adjacent activated electrode. Fig. 3 shows the operation of the gate for $X_1X_2 = 11$. When $t = 0$, two 1x droplets stay on the electrodes representing two inputs, while one 1x droplet stays on the electrode representing the reference port. Operations from $t = 1$ to 10 are the same as that in Fig. 2. Note that the splitting step in the experiment occupies five electrodes and lasts for three clock cycles, as shown from $t = 2$ to 4. This is because we want to ensure even and thorough splitting, to acquire two split droplets with equal volume. At $t = 11$, there is one 1x droplet on the electrode representing the output. Experimental results demonstrate the feasibility of the OR gate for different input values.

Fig. 1(b) illustrates the schematic of a 2-input microfluidic AND gate. The sequence of control voltages applied to each electrode is shown in Table 2. The delay of the AND gate is 5 clock cycles. Fig. 1(c) shows a microfluidic inverter. The sequence of actuation voltages applied on each electrode is shown in Table 2. The delay of the inverter is 9 clock cycles. Fig. 1(d) illustrates the schematic of a microfluidic XOR gate. The logic function of this XOR gate is as follows: $Z = X_1 \cdot \overline{X_2} + X_2 \cdot \overline{X_1}$. The sequence of control voltages applied to each electrode of the XOR gate is the same as that of the inverter. The delay of this XOR gate is also 9 clock cycles.

Table 2. Actuation voltage sequence for the AND gate and the inverter (the values for the inverter are shown in parentheses)

Clock	Electrode No.												
cycle	1	2	3	4	5	6	7	8	9	10	11	12	13
0	1(1)	1(0)	0(1)	F(1)	F(0)	F(F)	F(0)	0(F)	1(F)	(F)	(0)	(1)	(0)
1	0(1)	0(0)	1(0)	0(1)	F(0)	F(0)	F(1)	0(0)	1(F)	(F)	(0)	(0)	(0)
2	0(1)	1(0)	0(0)	1(1)	0(0)	F(1)	F(0)	0(1)	1(0)	(F)	(0)	(0)	(0)
3	F(1)	0(0)	0(F)	0(1)	1(0)	0(0)	F(0)	0(0)	1(0)	(F)	(1)	(0)	(1)
4	F(1)	F(0)	F(F)	0(0)	0(1)	1(0)	0(F)	0(0)	1(F)	(F)	(0)	(0)	(0)
5	F(1)	F(0)	F(F)	F(0)	0(0)	0(1)	1(0)	0(F)	1(F)	(F)	(0)	(F)	(F)
6	(1)	(0)	(0)	(F)	(0)	(0)	(1)	(0)	(F)	(F)	(0)	(0)	(F)
7	(1)	(0)	(0)	(F)	(F)	(0)	(0)	(1)	(0)	(F)	(F)	(0)	(0)
8	(1)	(0)	(0)	(F)	(F)	(0)	(1)	(0)	(1)	(0)	(F)	(0)	(0)
9	(1)	(0)	(0)	(F)	(F)	(0)	(1)	(0)	(0)	(1)	(F)	(0)	(F)

4 Potential Application of Microfluidic Logic

HIV test is integral to HIV prevention, treatment, and care efforts. The knowledge of an individual's HIV status is important for preventing the spread of this disease. Early knowledge of HIV status is also important for offering those who are HIV positive with medical care and services to improve quality of life [9]. Early diagnosis is important for effective treatments and to prevent transmission of HIV infection to other individuals.

A common test for HIV can be implemented on a digital microfluidic platform. Tests used for the diagnosis of HIV infection should achieve a high degree of both sensitivity and specificity. This is achieved by combining the screening assay and

the confirmatory assay. In the US, the enzyme-linked immunosorbent assays (ELISA) are commonly used for screening to look for antibodies to HIV, and the Western Blot procedure is commonly used for confirmatory assay. A positive ELISA must be used with a follow-up (confirmatory) test such as the Western Blot to make a positive diagnosis [8].

The ELISA test, on blood drawn from a vein, is the most common screening test used to look for antibodies to HIV. The results of the ELISA test, which are in the form of chromogenic, fluorogenic, or electrochemical signals, can be viewed by optical or electrochemical devices. The results of the ELISA test are qualitative, either positive or negative. If the result of the ELISA test is negative, there are no HIV antibodies in the blood sample, confirming that the individual is not infected with HIV. If the result of ELISA is positive, a follow-up (confirmatory) test such as the Western Blot must be used to make a positive diagnosis.

The results of Western Blot are analyzed in the following way: If no viral bands are detected, the result is negative. If at least one viral band is present for each gene-product group, the result is positive. Tests in which less than the required number of viral bands is detected are defined as indeterminate. The person who has the indeterminate result should be retested, as later tests may be more conclusive.

The microfluidic logic gates can be used to implement logic operations for the on-chip HIV test. Although the speed of microfluidic computing using microfluidic logic gates is much less than silicon-based computing devices, the microfluidic logic operations will enhance the on-chip HIV test through direct incorporation of computing functions on-chip with primary HIV test operations without the conversion between fluidic signals and electrical signals.

One logic operation is outlined here to evaluate the results of Western Blot. Assuming there are n gene-product groups (typically $n = 3$), we define $X_j = 1$ if there is at least one viral band for gene-product group j. We use two logic functions as follows.

$$Y = OR(X_1, X_2, \ldots, X_j, \ldots, X_n),$$
$$Z = AND(X_1, X_2, \ldots, X_j, \ldots, X_n).$$

If no viral bands are detected, then $Y = 0$, else $Y = 1$. If at least one viral band for each of the n gene-product groups is present, then $Z = 1$, else $Z = 0$. The results of Western Blot can be evaluated by the combination of Y and Z, as shown in Table 3.

Table 3. Result-evaluation table of Western Blot

Signal Y	Signal Z	Western Blot Result
0	0	negative
0	1	forbidden state
1	0	indeterminate
1	1	positive

5 Conclusions

Microfluidic logic gates have been proposed based on the digital microfluidic platform. Microfluidic AND, OR, NOT and XOR gates can be implemented through basic droplet-handling operations such as transporting, merging and splitting by using the principle of electrowetting-on-dielectric. Experimental results demonstrate the feasibility of the microfluidic logic gates for different input values. A potential application for microfluidic logic gates is to implement microfluidic logic operations for on-chip HIV test.

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