

3D CMOL Crossnet for Neuromorphic Network Applications

Kevin Ryan, Sansiri Tanachutiwat, and Wei Wang

College of Nanoscale Science and Engineering at SUNY Albany,
Albany, 12222 New York, USA
{kryan, stanachutiwat, wwang}@uamail.albany.edu

Abstract. In this work, a novel 3D CMOL crossnet structure is introduced by combining two leading technological concepts for future nanoelectronic neuromorphic networks: CMOL crossnet and 3D integration. By implementing CMOL crossnet into the third dimension, the proposed 3D CMOL crossnet not only maintains the high-speed and high defect-tolerant properties of the CMOS-nano hybrid CMOL hardware system, but also provides efficient fabrication and assembly processes with a much higher density than the original CMOL crossnet. Furthermore, this study focuses on the development of multivalued synapses and efficient communication methods between CMOS and nanodevices. Preliminary results demonstrate that the structure can utilize the advantages of high performance synapses and stable analog CMOS somas in three dimensions. Therefore, the proposed 3D CMOL crossnet structure has a huge potential to become an efficient 3D hardware platform to build neuromorphic networks that are scalable to biological levels.

Keywords: CMOS-Nano Hybrid System, CMOL, Crossnet, Neuromorphic Network, 3D IC.

1 Introduction

For many years, researchers and programmers have been trying to mimic the brain's neuromorphic network (NN) in software, and in this task they have been successful [1], [2]. Even though, the complexity of the brain's functions have been captured, its efficiency and power at executing these tasks is still an alluring goal. Utilizing today's computer architecture, the software solutions based on a number of enormous supercomputers can not match the brain's speed and processing power. In order to provide unparalleled computational efficiency and density, the reconfigurable hardware platforms might be a promising solution to mimic the brain's structure [3-5].

Recent studies [6-11] demonstrated that the CMOS-nano hybrid technology can provide an efficient hardware platform to build a family of neuromorphic networks. Based on a hybrid technology, the CMOS parts will implement neural cell bodies (somas) and the nanodevices with reconfigurable capabilities can be used as synapses. The dendrites and axons will be implemented by interconnects or nanowires. This CMOS-nano hybrid neuromorphic network can utilize the advantages of both CMOS and nanodevices.

One key challenge of CMOL crossnet is how to efficiently establish communication between CMOS and nanodevices. As shown in Fig. 1a, the CMOL crossnet requires special pins with different heights to connect CMOS and nanodevices, which are difficult to fabricate. Since each nanowire segment requires one pin, millions of these special pins are required, which may not be feasible to build.

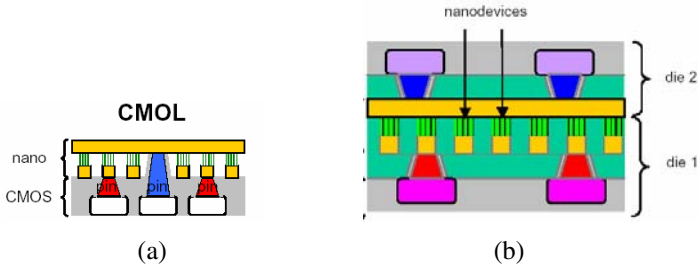


Fig. 1. (a) The CMOL structure with the special pins to connect CMOS and nanodevices [6]. (b) 3D CMOL without the special pin requirement [12].

In order to tackle the challenge of CMOL crossnet, we present our recent research results in developing efficient 3D hybrid neuromorphic network systems. We introduce a 3D CMOL crossnet concept to improve fabrication process, and performance of CMOL crossnet.

2 3D CMOL Crossnet

To ease the fabrication process especially in the area of pin placement and connections, the 3D CMOL crossnet was developed by sandwiching the nanodevices between two separate layers of CMOS (Fig. 1b). Besides the fabrication advantages of this configuration it also doubles the CMOS area and therefore increases the soma density of the architecture. On the other hand, 3D CMOL crossnet will present some design challenges that need to be overcome.

In the brain a soma is the logical unit between the axons and dendrites that controls signal propagation. The soma design presented by Likharev is shown in Fig. 2a and naturally assembles into a matrix type of architecture when put into an array. A known benefit of this design is the negative axon-dendrite connection that will always send the opposite signal than its positive counterpart because of the electrical properties of the diode. Since the somas are not able to connect to both layers of nanowires on the crossbar we must take the input and output solely from the vertical or horizontal wires as shown in Fig. 2b. With this arrangement there will be no natural inverse voltage running through the wires, so an inverter has been added before the negative pole of the amplifier to correct the problem.

The final issue to discuss regarding the crossbar structure is the existence of axon-axon and dendrite-dendrite connections. These extra connections which are not found in the brains neuromorphic network are handled quite effectively by the electrical properties of the crossbar. Because of low impedance in the soma's amplifier and

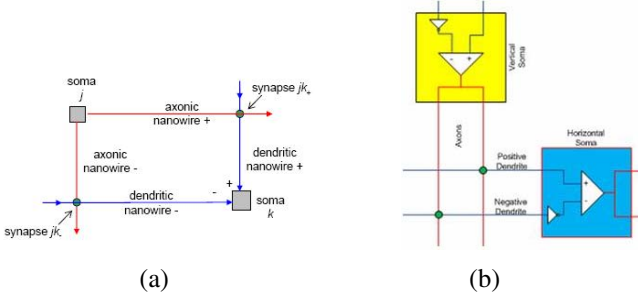


Fig. 2. (a) General soma-soma connection as proposed by Likharev (adapted from [7]). (b) Revised 3D CMOL soma-soma connection.

high voltage carried in the axonic nanowires, the axon-axon connections can be disregarded. The dendrite-dendrite connections are not an issue as long as the dendrite voltages are kept lower than the axons hence it will not disrupt the axon's signal already in the wire [8].

Based on the 3D CMOL crossnet structure, we present various designs of neuromorphic networks in this section. These designs tailor the 2D CMOL designs to suit the 3D CMOL crossnet structures. There are two main structures with different variations that can be used to pattern the somas; they are called Alternating FlossBar (Fig. 3a) and Alternating InBar (Fig. 3b). These designs follow an alternating pattern because each soma can only connect to a soma of the opposite type via the synapses. Finally to increase the synapse density we have developed the Cut Alternating FlossBar (Fig. 3c) which makes use of every nanowire junction as a synapse.

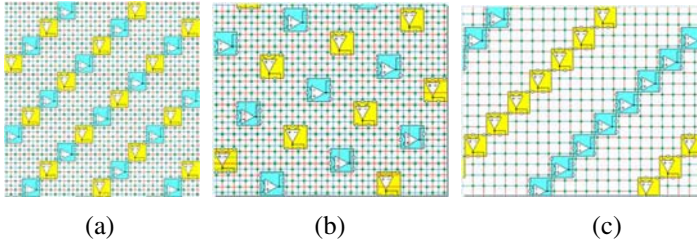


Fig. 3. (a) Alternating FlossBar. (b) Alternating InBar. (c) Cut Alternating FlossBar.

3 Performance Evaluation

In order to evaluate the performance of the proposed 3D CMOL crossnet, we carry out an analysis in terms of area, speed, and power consumption. Note that for simplicity, this analysis does not consider defects and process variations of devices and is not dependent on any specific soma layout.

Table 1 summarizes the estimated implementation results of 2D CMOL crossnet and 3D CMOL crossnet. As shown in Table 1, the proposed 3D CMOL crossnet circuits provide a 2X area improvement over the 2D CMOL crossnet designs with

similar operational speed. This is due to 3D CMOL's structure significantly reducing the footprint and logic stages. Also, interconnects and routing of the circuits will be significantly simplified. The 3D CMOL structure can efficiently partition and interconnect lengths and routing complexity to achieve high performance. The average dynamic power of the 3D CMOL designs is a little higher than the original crossnet designs. The short interconnect length of the 3D structure will reduce the dynamic power, but this effect is counteracted by the large capacitance of the nanowire crossbar with its very high density.

A significant advantage of the 3D CMOL crossnet in terms of performance is the density increases compared to the 2D CMOL crossnet. Due to the significant density improvement, this proposed technology would provide huge potential to build future generations of NN applications. However, the challenge of 3D CMOL crossnet lies in the power and thermal management due to its high power density values.

Table 1. Table Performance comparison of 3D CMOL crossnet and 2D CMOL crossnet for spiking and non-spiking models

Non-spiking model	Area (Processing nodes per 858 mm ²)	Speed	Power
CMOL crossnet [11]	1716	50 Hz 140Hz 482 Hz	1.4W
3D CMOL crossnet	3832	<50 Hz <140Hz <482 Hz	<2.8W

Spiking model	Connectivity	Area (Processing nodes per 858 mm ²)	Power
CMOL crossnet [11]	0.1	276	1.8
3D CMOL crossnet	0.1	552	<3.6
CMOL crossnet [11]	0.01	276	2.7
3D CMOL crossnet	0.01	552	<5.4
CMOL crossnet [11]	0.001	276	6.2
3D CMOL crossnet	0.001	552	<12.4

4 Conclusion

In this paper, we have carried out a preliminary study covering the architecture and circuit design of 3D CMOL crossnet. By utilizing high-density nanodevices and high-performance CMOS analog circuits in three dimensions, we can achieve an efficient hardware platform to build neuromorphic network systems. In the future, this CMOS-nano-CMOS one-stack structure can be extended to mutli-stack structures, by bonding several stacks together in a back-to-back manner and connecting them with through-silicon-vias. Such a 3D structure can open up possibilities to develop more complex (hierarchical or modular) neuromorphic systems and brain-like machines. In fact, the

human brain essentially is a 3D structure, which can be mimicked by the multi-stack 3D CMOL crossnet.

It is noted that more knowledge of our brain is required to emulate its functionality for advanced intelligent tasks. Recently, neurobiological research has found huge amounts of valuable information related to the brain's structure. Such developments may shed light on future 3D CMOL research. We expect that incorporating the new neuromorphic network research results with the development of 3D CMOL crossnet, may well lead to an innovation or technology breakthrough to construct computers that can match the power of the brain.

Acknowledgments. This work has been supported in part by the AFSTTR and MARCO (via IFC Center). Useful discussions with K. K. Likharev are gratefully acknowledged.

References

1. Varshney, L.R., Sjostrom, P.J., Chklovskii, D.B.: Optimal information storage in noisy synapses under resource constraints. *Neuron*. 52(9), 409–423 (2006)
2. Wen, Q., Chklovskii, D.B.: Segregation of brain into gray and white matter: a design minimizing conduction delays. *PLOS Computational Biology* 1(7), 617–639 (2005)
3. Berger, T.W., et al.: Brain-implantable biomimetic electronics as the next era in neural prosthetics. *Proceedings of the IEEE* 89(7), 993–1012 (2001)
4. Indiveri, G., Chicca, E., Douglas, R.: A VLSI array of low-power spiking neurons and bistable synapses with spike-timing dependent plasticity. *IEEE Transactions on Neural Networks* 17(1), 211–221 (2006)
5. Vogelstein, R.J., Mallik, U., Vogelstein, J.T., Cauwenberghs, G.: Dynamically reconfigurable silicon array of spiking neurons with conductance-based synapses. *IEEE Transactions on Neural Networks* 18(1), 253–265 (2007)
6. Strukov, D.B., Likharev, K.K.: A reconfigurable architecture for hybrid CMOS/nanodevice circuits. In: *FPGA 2006*, pp. 131–140 (February 2006)
7. Türel, Ö., Lee, J.H., Ma, X., Likharev, K.K.: Nanoelectronic neuromorphic networks (crossnets): new results. In: *Proc. IJCNN 2004*, pp. 389–394 (2004)
8. Türel, Ö.: Devices and circuits for nanoelectronic implementation of artificial neural networks. Ph. D Thesis (2007)
9. Türel, Ö., Lee, J.H., Ma, X., Likharev, K.K.: Neuromorphic Architectures for Nanoelectronic Circuits. *Int. J. of Circuit Theory and Applications* 32, 277–302 (2004)
10. Lee, J.H., Likharev, K.K.: Defect-Tolerant nanoelectronic pattern classifiers. *Int. J. of Circuit Theory and Applications* 35, 239–264 (2007)
11. Gao, C., Hammerstrom, D.: Cortical Models Onto CMOL and CMOL-Architectures and Performance/Price. *IEEE Trans. Circuit and System I* 54(11) (November 2007)