A Buck-Boost Multilevel Inverter for PV Systems in Smart Cities

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Abstract. This paper proposes a new buck-boost multilevel inverter topology, which is named as a hybrid quasi-Z-source network multilevel inverter, for photovoltaic systems in smart cities. This topology employs an impedance source network and a high frequency three-level switching unit connected to the low frequency single phase inverter. In comparison with other quasi-Z-source network multilevel inverter topologies, the proposed topology uses a lower number of circuit components and more reliable operation. In addition, an effective modulation technique based on phase-shifted disposition scheme is introduced to control the shoot-through state for both boost and buck states of the output voltage. The operating principle of the proposed topology is analyzed in detail. Both simulation and experimental results are carried out to validate the performance of the proposed topology.

Keywords: Multilevel inverters · Quasi-Z-source inverter
Boost control method · Pulse width modulation (PWM)

1 Introduction

Smart city is a combination of diverse technologies to decrease their environmental influences and create citizens better lives. Increasing energy efficiency of building installation and using of renewable energy resources cover remaining energy needs [1, 2]. In photovoltaic (PV) systems, the output voltage of a PV cell widely varies with irradiation and temperature. Therefore, the conventional voltage source inverter (VSI) cannot deal with this change because the VSI is a buck inverter. Normally, a dc-dc boost converter is required to obtain the desired AC output voltage. However, the additional boost converter increases the cost and decreases the efficiency of the overall system. To overcome limitations in the VSI, the Z-source inverters (ZSI) and quasi-Z-source inverter (qZSI) proposed in [3, 4]. The qZSI topologies have advantages over the ZSI topologies such as lower voltage stress on the capacitors and continuous input current. Because of these benefits, it is more attractive to industrial applications such as electric vehicle or PV systems [5, 6].

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Recently, multilevel inverters have been selected as a very attractive solution for medium-voltage high-power applications. They allow to generate a better output voltage with low distortion AC waveform by increasing the number of voltage levels and share the total dc voltage between cascaded switching devices [7, 8]. A two-stage conversion configuration with buck-boost ability will make more complex system and higher cost and trends to decrease the system reliability and efficiency.

In order to obtain the buck-boost function with a single-stage power conversion, the combination of advantages of both the impedance source networks and various multilevel inverters have been introduced in [9–12]. Three-level Z-source neutral point clamped (NPC) topology using two Z-source networks (ZSNs) are proposed in [9] and five-level Z-source NPC with two ZSNs is presented in [10]. These Z-source NPC topologies can decrease the system cost due to the lower number of impedance networks and dc voltage sources. The cascaded ZSN using two switching devices and one H-bridge unit proposed in [11]. In this topology, the number of switching devices can be reduced with respect to the conventional topology. However, two separate ZSNs and two separate dc sources are required in order to generate the output voltage with three voltage levels.

An integration of the quasi-Z-source network (qZSN) and the cascaded multilevel inverter is studied in [12]. One dc source and one qZSN are used for each H-bridge unit, therefore, many passive components are required in the qZSN. A single phase three-level NPC qZSN inverter is proposed in [13, 14]. It uses two symmetrical qZSNs fed from one dc source with a single phase three-level NPC inverter. Many diodes and switching devices are used that will increase the cost and size and reduce the reliability. In addition, if a higher number of level is required, the control method and balancing of capacitor voltage become more complex.

In this paper, the buck-boost three-level inverter is presented. The inverter is a combination of two qZSNs and a high frequency (HF) three-level switching unit connected to the low frequency (LF) single phase inverter. In this combination, the number of circuit components is reduced, the reliable operation is improved, and continuous input current is obtained. Moreover, an effective modulation technique based on a phase-shifted disposition (PSD) scheme is introduced to control the shoot-through states. The modified modulation method can be easily inserted the upper-shoot-through (UST) and lower-shoot-through states (LST) into the traditional sine modulation technique, therefore, offering a simple implementation. The performances of the proposed topology are verified by both in simulation and through experimental results.

2 Operating Principle of the Proposed Three-Level Inverters

2.1 The Proposed Topology

The power circuit of the proposed inverter is described in the Fig. 1. This inverter uses an impedance network to connect a three-level pulse width modulation (PWM) switching unit and an H-bridge unit with low switching frequency. The impedance source network consists of two identical qZSNs with a common point

between two capacitors C_1 and C_2 to provide a neutral point of the topology [14]. The high frequency switches S_1 to S_4 are used as a PWM switch in order to provide the desired output voltage and the low frequency switching unit S_5 to S_8 are controlled to generate the polarity of the output voltages [15]. The qZSN is used for boosting the dc input voltage V_{in} to the higher dc-link voltage v_i. Due to the symmetrical qZSN, we can obtain $L_1 = L_4$, $L_2 = L_3$, $C_1 = C_2$ and $C_3 = C_4$. As a result, the corresponding voltages are $v_{L1} = v_{L4}$, $v_{L2} = v_{L3}$, $V_{C1} = V_{C2}$ and $V_{C3} = V_{C4}$.

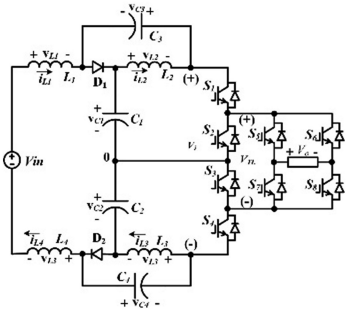


Fig. 1. Single phase three-level qZSN inverter

The operating states of the proposed inverter can be simplified into shoot-through state and non-shoot-through state. The operating principle of the proposed inverter is only discussed when the positive half of the output voltage, in which two switches (S_5, S_8) are turned on. The negative half-cycle of the output voltage with two on switches (S_6, S_7) can be similarly derived based on the previous analysis.

2.2 Shoot-Through State

The proposed inverter uses two shoot-through state types to boost the input voltage to a higher voltage value. Figure 2 describes these shoot-through states, at which the upper shoot- through state shows in Fig. 2(a) and lower shoot-through state shows in Fig. 2(b).

In the UST state for T_{UST} interval of total shoot-through time T_{SH}, three switches (S_1, S_2, and S_4) are turned on, diode D_1 is also connected, and D_2 is disconnected. The L_2 inductor stores the energy from capacitor C_1 through S_1 and S_2. In the LST state for T_{LST} interval of total short-through time T_{SH}, three switches (S_1, S_3, and S_4) are turned on, diode D_1 is disconnected, and D_2 is connected. The L_3 inductors store the energy from capacitor C_2 through S_3 and S_4. The positive half-cycle of the output voltage is provided by two switches (S_5, S_8).

The relative voltage equations in the UST can be represented as

$$v_{L1} = v_{L4} = \frac{1}{2}(V_{C3} - V_{C2} + V_{in}) \tag{1}$$

$$v_{L2} = V_{C1} \tag{2}$$

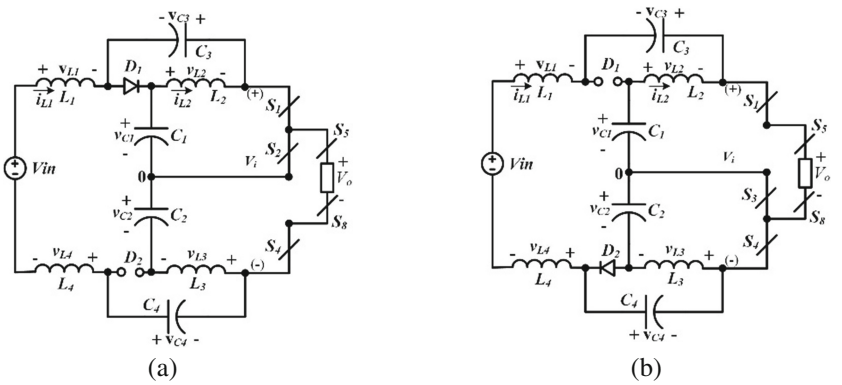


Fig. 2. Equivalent circuits of the shoot-through states: (a) upper shoot-through state, (b) lower shoot through state.

$$v_{L3} = V_{C4} \tag{3}$$

$$v_i = -(V_{C2} + V_{C4}) \tag{4}$$

The corresponding voltage equations of the LST state can be given as

$$v_{L1} = v_{L4} = \frac{1}{2}(V_{C4} - V_{C1} + V_{in}) \tag{5}$$

$$v_{L2} = V_{C3} \tag{6}$$

$$v_{L3} = V_{C2} \tag{7}$$

$$v_i = (V_{C3} + V_{C1}) \tag{8}$$

2.3 Non-Shoot-Through State

In the non-shoot-through state for the interval of Ta, the proposed inverter operates under the same operation principle of the inverter proposed in [15]. During the non-shoot-through state, both diodes D_1 and D_2 are on. The non-shoot-through state is classified by active state 1 (A-1), active state 2 (A-2), active state 3 (A-3), and null state (NS). The equivalent circuits of three active states and a null state are shown in Fig. 3. In the active state 1, as shown in Fig. 3(a), S_1 and S_4 are turned on. In this state, the peak dc-link voltage $\hat{v}_i$ can be obtained by adding the input voltage and four inductive voltages. In the active states 2 and 3, as shown in Fig. 3(b) and (c), a pair of switches (S_1, S_4) and (S_2, S_3) are turned on, respectively. Both these active states have the same dc-link voltage with the shoot-through states but they are a half of the peak dc-link voltage. The load terminal has a zero voltage in the null state.

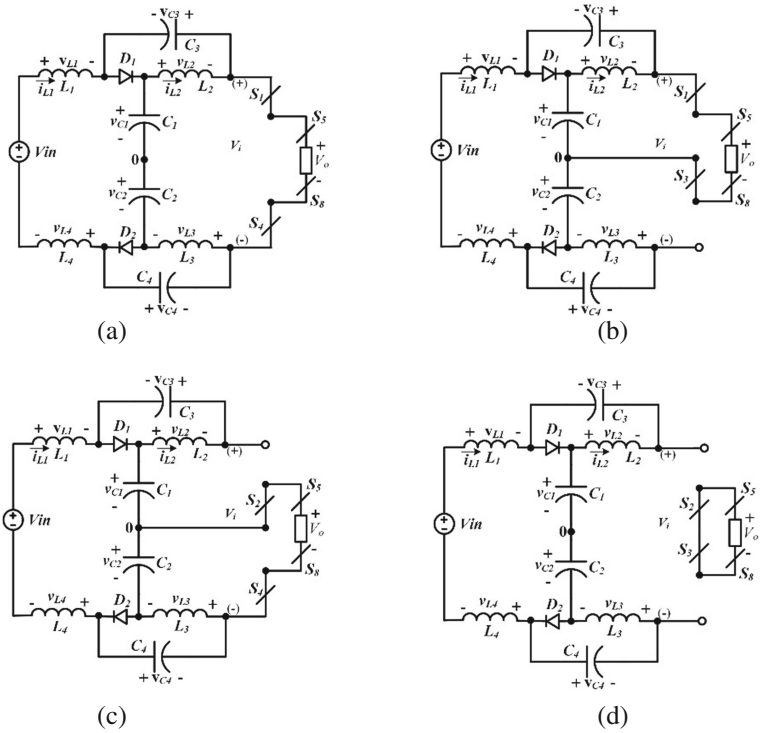


Fig. 3. Equivalent circuits of the non-shoot-through states: (a) active state 1, (b) active state 2, (c) active state 3, (d) null state.

The inductive voltage and dc-link voltage in the non-shoot through states are given as follows

$$v_{L1} = v_{L4} = \frac{1}{2}(V_{in} - 2V_{C1}) \tag{9}$$

$$v_{L2} = -V_{C3} \tag{10}$$

$$v_{L3} = -V_{C4} \tag{11}$$

$$v_i = V_{C1} + V_{C2} + V_{C3} + V_{C4} \tag{12}$$

2.4 Boost Capability

Applying the volt-second balance principle on the inductor L_2, we have

$$V_{C3} = \frac{D}{2-D}V_{C1} = \frac{D}{2-D}V_{C2} \tag{13}$$

Where $D = T_{ST}/T_s$ is the shoot-through duty cycle, and TST is the shoot-through time during switching period T_s.

Similarly, applying the volt-second balance principle on the inductor L_1, we get

$$V_{C1} = V_{C2} = \frac{D}{2 - D} V_{in} \tag{14}$$

Substituting (14) to (13), the capacitor voltage of C_3 and C_4 can be derived as follows

$$V_{C3} = V_{C4} = \frac{D}{4 - 4D} V_{in} \tag{15}$$

The peak dc-link voltage across the main inverter expressed in (8) and can be expressed as follows

$$\hat{v}_i = \frac{1}{1 - D} V_{in} \tag{16}$$

A boost factor, which is expressed as a ratio of the peak dc-link voltage and the input voltage, can be calculated as

$$B = \frac{\hat{v}_i}{V_{in}} = \frac{1}{1 - D} \tag{17}$$

Figure 4 illustrates the plot of the boost factor of the inverter with a variation of duty cycle.

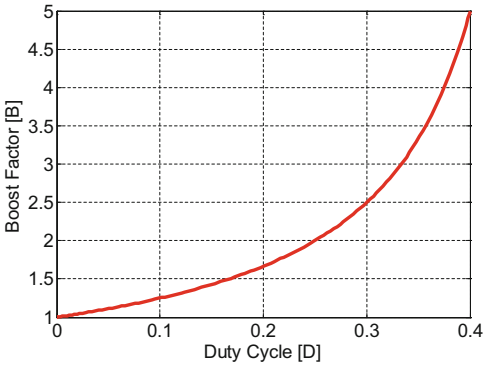


Fig. 4. Boost factor for different duty cycle.

3 Comparison of Proposed Topology with Other qZSN Topologies

The number of circuit components is used for the proposed topology is compared with different qZSN topologies. Table 2 illustrates a comparison between the proposed topology with different three-level topologies.

4 Boost Modulation Techniques

Several boost modulation techniques for the Z-source NPC [16–18] and the qZSN multilevel inverter [19], are introduced to improve the output performance such as harmonic distortion or reduced switching losses. In the paper, a proper boost control strategy for the proposed inverter is presented in Fig. 5. It is a modified modulation technique based on PSD method [20].

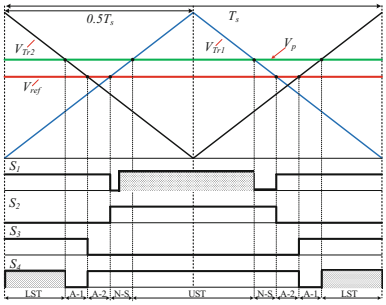


Fig. 5. Switching patterns in one switching period

The proposed technique uses two triangular carriers, where each carrier is phase shifted by 180 from its adjacent carrier. These carriers are compared with the sinusoidal reference signal V_{ref} and the straight line signal V_p, in order to generate the desired switching patterns for four switches S_1, S_2, S_3, S_4. Two switches (S_5, S_8) are turned on during the reference signal V_{ref} is positive and two switches (S_6, S_7) are turned on during the reference signal V_{ref} is negative. An output voltage is five voltage levels when the modulation index M is higher than 0.5. One switching pattern for one switching period is shown in Fig. 5. The upper and lower shoot-through states can be achieved by comparing the straight line signal V_p with the two carrier signals V_{tr1} and V_{tr2}, respectively. During one switching period, two shoot-through states and non-shoot-through states are symmetrically generated.

Table 1 summarizes the operating states, output voltage levels, and capacitor voltages. From the table, the UST and A-2 states are received energy from the capacitor voltage on V_{C1}. While the capacitor voltage V_{C2} is used for the LST and A-3 states. The two series capacitor voltage V_{C1} and V_{C2} are used for the A-1 mode. During one fundamental period, the capacitor voltage on C_2 and C_2 makes the different voltage

Table 1. Comparison of the number of circuit components

Topologies	HF switches	LF switches	Diodes	DC sources	Inductors	Capacitors
Cascaded qZSN	8	0	2	2	4	4
qZSN NPC topology	8	0	6	1	4	4
Proposed topology	4	4	2	1	4	4

Table 2. Switching patterns and output voltage

Operating modes	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_o	Capacitor voltages
A-1	1	0	0	1	1	0	0	1	$+\hat{v}_i$	$V_{C1} + V_{C2}$
UST	1	1	0	1	1	0	0	1	$+\hat{v}_i/2$	V_{C1}
LST	1	0	1	1	1	0	0	1	$+\hat{v}_i/2$	V_{C2}
A-2	1	0	1	0	1	0	0	1	$+\hat{v}_i/2$	V_{C1}
A-3	0	1	0	1	1	0	0	1	$+\hat{v}_i/2$	V_{C2}
NS	0	1	1	0	1	0	0	0	0	–
NS	0	1	1	0	0	1	1	0	0	–
A-3	1	0	1	0	0	1	1	0	$-\hat{v}_i/2$	V_{C2}
A-2	0	1	0	1	0	1	1	0	$-\hat{v}_i/2$	V_{C1}
LST	1	0	1	1	0	1	1	0	$-\hat{v}_i/2$	V_{C2}
UST	1	1	0	1	0	1	1	0	$-\hat{v}_i/2$	V_{C1}
A-1	1	0	0	1	0	1	1	0	$-\hat{v}_i$	$V_{C1} + V_{C2}$

levels of the output voltage. Due to the symmetrical characteristic of the operating states of the modified PSD technique, the capacitor voltages V_{C1} and V_{C2} can be automatically balanced during one switching period.

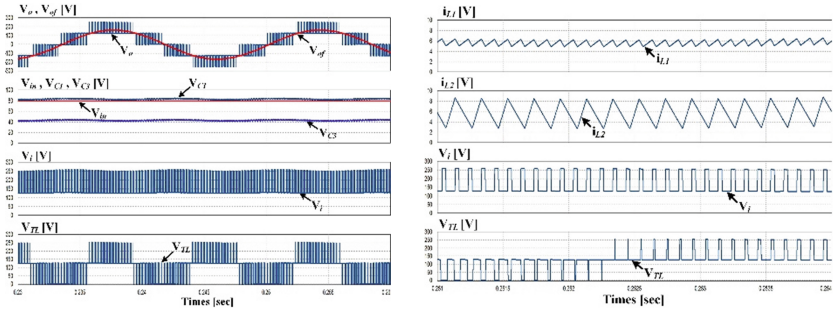
5 Simulation and Experimental Results

5.1 Simulation Results

In order to verify the theoretical results of the proposed topology, PSIM simulation studies are performed. The DC input is V_{in} = 80 V, and the switching frequency is f_s = 5 kHz. The simulation parameters are selected as follows:

(1) Impedance network: $L_1 = L_2 = L_3 = L_4$ = 1 mH, $C_1 = C_2 = C_3 = C_4$ = 1 mF
(2) LC output filter: L_f = 0.6 mH, C_f = 100 μF
(3) Resistive load: R_L = 30 Ω

Figure 6 shows the simulation results of the proposed topology when M = 0.65 and D = 0.35. In the Fig. 6(a), the peak dc-link voltage V_i is boosted from V_{in} = 80 V to 266 V. The capacitor voltage V_{C1} and V_{C3} are 86 V and 46 V, respectively. The AC output voltage before filter has three voltage levels, and the peak AC output voltage after filtering is V_{of} = 123 V. From the Fig. 6(b), the inductor current i_{L1} increases in the shoot-through state and decreases in the non-shoot-through state. The inductor



(a) (b)

Fig. 6. Simulation waveforms of the proposed inverter when M = 0.65 and D = 0.35.

current i_{L2} has a higher ripple than the i_{L1} current. The output voltage of the three-level PWM switching unit V_{TL} is a dc voltage with three voltage levels.

For illustrating the boosting capability in the transient condition, Fig. 7 shows the dc-side response where the shoot-through time is increased from 0.2 to 0.35. From top to bottom, the AC output voltage before filtering and after filtering, DC-link voltage V_i, the capacitor voltage V_{C1} and V_{C2}, and the input voltage V_{in}. At 0.2 s the D has step change and the peak DC-link voltage would change from V_i = 130 V to 265 V, capacitor voltages V_{C1} = 53 V to 87 V, and V_{C3} = 13 V to 47 V, finishing the step response at the steady state. The RMS output voltage value increases from V_{of} = 75 V to 87 V.

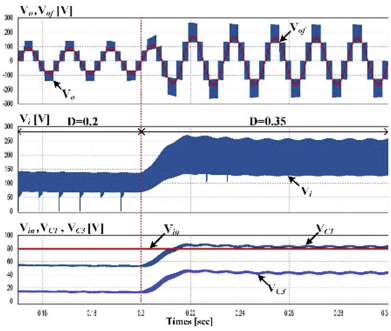


Fig. 7. Transient simulation of the proposed inverter when duty cycle changes from D = 0.2 to D = 0.35 and M = 0.65.

5.2 Experimental Results

In order to validate the analysis, a single phase three-level inverter prototype with a high performance DSP TMS320F28335 has been built in the laboratory for verifying the theoretical analysis and the simulation results. The experimental parameters are used the same as the simulation parameters.

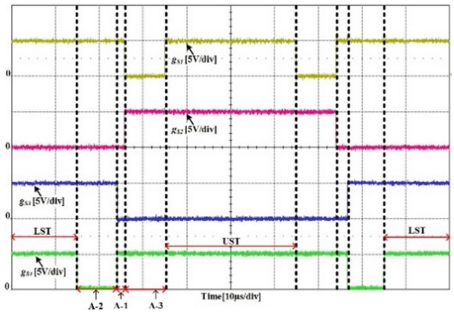
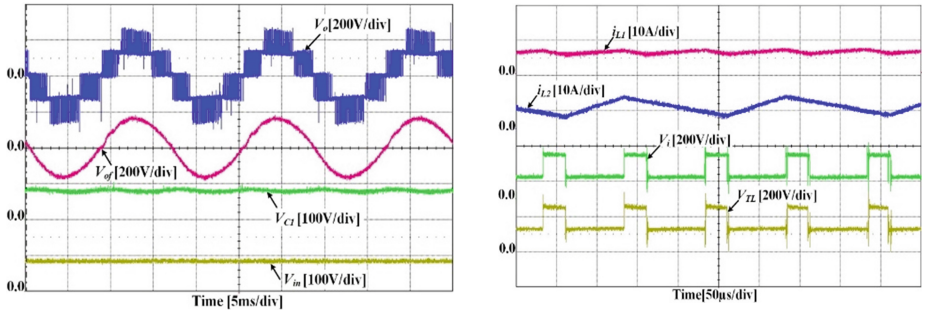


Fig. 8. Gating signal waveforms of S_1, S_2, S_3, and S_4

Figure 8 shows the gating control signals of switching devices $S_1 - S_4$ for one switching period. As the mentioned analysis, two shoot-through states and three active states are distributed symmetrically in one switching period.

For illustrating the boost capability, Fig. 9 shows the experimental results when M = 0.65 and D = 0.35. In the Fig. 9(a), the RMS value of the output voltage is V_{of} = 86 V and the capacitor voltage of C_1 is V_{C1} = 86 V. In Fig. 9(b), the waveforms from top to bottom are the inductive currents i_{L1} and i_{L3}, dc-link voltage V_i, and the output voltage of three-level switching unit V_{TL}. The i_{L1} current is smoother than the i_{L3} current and the V_{TL} voltage has three voltage levels. The peak value of DC-voltage is V_i = 255 V, which is lower than that of the simulation results because of the effects of the parasitic components and the average inductor currents i_{L1} = 6 A and i_{L2} = 4 A.

The measure efficiency curve varied with the duty cycle D of the proposed topology is shown in Fig. 10. It can be clearly seen that the efficiency of the proposed inverter will go down when increasing the duty cycle. From this result, it illustrates that the power losses are proportional to the boost capability of the inverter because the stronger boost factor corresponding to the higher current through the inductors and semiconductor devices. A higher efficient design can be made by optimal impedance network and switching devices.



(a) (b)

Fig. 9. Experimental waveforms of the proposed topology when M = 0.65 and D = 0.35

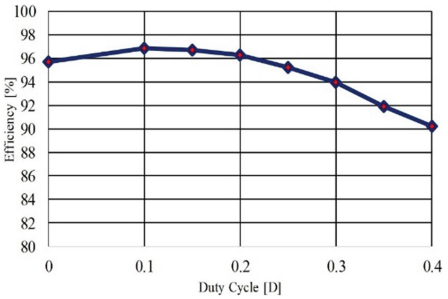


Fig. 10. Measured efficiency against duty cycle for the proposed topology

6 Conclusions

A buck-boost three-level inverter for the renewable energy systems in the smart cities has been proposed. The proposed inverter uses the qZSN to couple with the three-level switching unit. The polarity of the output voltage is produced by the LF single phase inverters. The main advantages of the proposed topology consist of continuous input current, lower circuit components, and higher operating reliability. In addition, a modified boost control technique is also presented to effectively control the shoot-through state. The operating principle and steady-state analysis are carefully performed. The simulation results show a good agreement with the theoretical analysis validating the exact operation of the proposed topology. The experimental results and the measured efficiency are obtained from the experimental prototype in the laboratory. Based on the benefits of the proposed inverter that will make it a competitive solution for renewable energy systems such as PV and fuel-cell.

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