A 100 MHz SRAM Design in 180 nm Process

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Abstract. With the development of integrated circuit, SoC systems are more and more used in products. Memory is an important part of SoC, SRAM design is a key research area. In this paper, based on ASIC design methodology, 2 K-bits SRAM is designed. A 6T-SRAM memory cell is designed and simulated with circuit level to improve reliability. The memory cell is used to construct the storage array, which are the word line 32 bits and the bit line 8 bits. Then, the SRAM peripheral circuit is designed and simulated by using SMIC 0.18 μm process, including the data input/output buffer circuit, clock circuit, address decoding circuit, data read/write circuit and sense amplifier. The structure, function and performance of latch type sense amplifier are analyzed emphatically. The simulation results demonstrate that the function of SRAM is verified correctly. The clock frequency of the SRAM can reach 100 MHz.

Keywords: Static random access memory · Memory array · Peripheral circuits

1 Introduction

With the rapid development of digitalization process, the information industry is going into the era of large data. SoC chip has become the key of information and data processing. The data storage in SoC is an important part. In order to solve the storage problems of SoC data storage, improve the working performance of SoC processor, and reduce the speed gap between processor and external memory, memory hierarchical technology is adopted in this paper. Static random access memory (SRAM) with high speed and low capacity is used as the key technology to solve the above problems. In this paper, with the analysis of the internal working mechanism about SRAM, the design methodology based on ASIC is adopted, in order to achieve 256 × 8 bytes.

A variety of design implementation and improvement schemes are proposed for SRAM. A novel power gated 9T SRAM cell is proposed, which uses read decoupling access buffers and power gated transistors to perform reliable read and write operations [1]. A bit line equivalent scheme is proposed to eliminate the leakage dependence of the data pattern. Thus, the read bit line sensing and its stability to the process, voltage and temperature variations are improved [2]. A 6T SRAM operating down to near threshold regime is presented [3]. A dual-port spin-orbit torque magnetic RAM for on-chip caching applications with reduced power consumption is proposed to reduce the impact of write delay on performance [4].

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2 SRAM Cell Structure

SRAM refers to a memory capable of accessing any unit in the memory array, which can perform data writing or data reading operations within an applicable range of address for multiple of cycles. The SRAM structure mainly includes the storage array, decoding circuit, clock circuit and data read/write control circuit, and so on. A storage array is a key part, which is electrically interconnected by the memory cell in accordance with certain rules. The decoding circuit is used to process the address information to select the particular cell. The clock circuit provides a series of working clock pulses for the operation of the peripheral circuit. Sense amplifier circuit is used to increase the speed of reading the stored data from SRAM array.

The basic memory cell of SRAM is shown in Fig. 1. It is composed of a pair of inverters and the pass transistors, which are connected in a cross-coupled manner. The output of an inverter becomes the input of the other inverter, and vice versa.

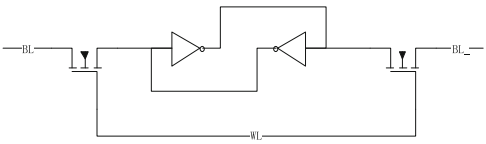

Fig. 1. Static memory cell based on 6T.

The simulation circuit for the 6T static memory cell is shown in Fig. 2. The data reading/writing and data holding for the 6T static memory cell are controlled by the BL_CTR_W, BL_CTR_R switches signal on the control bit line and the word line switch signal WL respectively. When the word line signal is valid, BL_CTR_W signal responds. If BL_CTR_R signal is invalid, the DC voltage source and bit line cascade are controlled by BL_CTR_W signal. By simulating the charging and discharging for the storage node on the bit line capacitor, the data is in the write state.

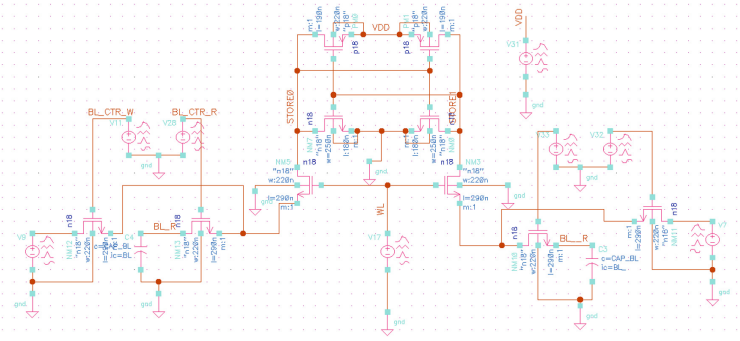

Fig. 2. The simulation circuit for the 6T static memory cell.

The simulation result for the 6T static memory cell is shown in Fig. 3.

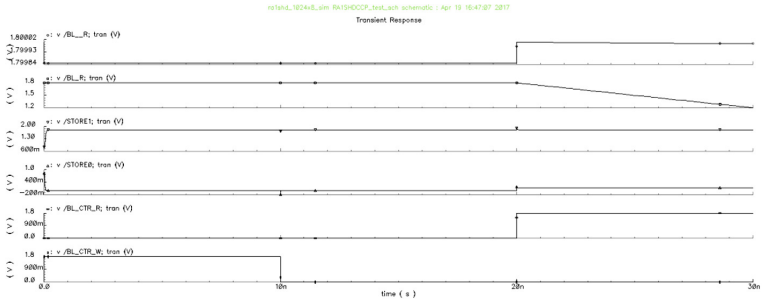

Fig. 3. The simulation result for the 6T Static memory cell.

Data can be read through the STORE0 and STORE1 signals to verify that the data has been written successfully. When the word line signal is invalid, the switch controlled by the BL_CTR_W and BL_CTR_B signals is disconnected from the memory node, which is the data holding state at this time. The data signal on the memory node can be latched properly if the STORE0 and STORE1 signals can be read out.

When the word line signal is valid, BL_CTR_W signal is invalid and BL_CTR_R signal is valid. At this point, the BL_CTR_R signal controls the pre-charged capacitor and the memory node for cascade connection. It is the data reading process through the BL_R and BL_R signals. The correct voltage difference is generated successfully on the two bit line capacitors, and the data is successfully read out.

3 Memory Array

The static memory cells are arranged and joined together to construct a memory array, as shown in Fig. 4. Each row of memory cells shares a word line WL. The static memory cells on each column share a pair of the bit lines BL and BL_. The selection signal of the word line and bit line is generated by the decoding circuit according to the address.

In the intersection selection of rows and columns, the position of intersection points can be obtained. It is the memory cell corresponding to the address information. By combining the memory array with the decoding circuit, the memory cell can be positioned quickly according to the address information. The corresponding operation of the memory cell is performed according to the data changes on the bit lines.

The address information used to locate the memory cells in the storage array is transmitted by code, which could reduce the number of inter-chip or on-chip interactive connections. Because binary code has area validity and easy implementation within the circuit, most of the code which adopted in CMOS memory is using the binary form. In a memory array, address information used to locate the memory cell is transmitted through code for reducing the number of interconnects for between chips or internal chip. Most of the code used in CMOS memory is binary encoding, because binary code can optimize chip area and easy to implement inside the integrated circuit.

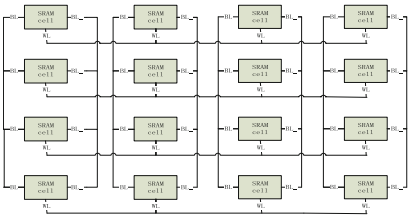

Fig. 4. Storage array diagram of 4 × 4.

The input signal used in the experimental simulation is shown in Fig. 5. The input patterns are 00–11 four bit signals for the address input ports ADD0 and ADD1 in the 2–4 decoder circuit. A signal is input at each interval of 5 ns. ADD0 and ADD1 are the lowest and highest addresses, respectively.

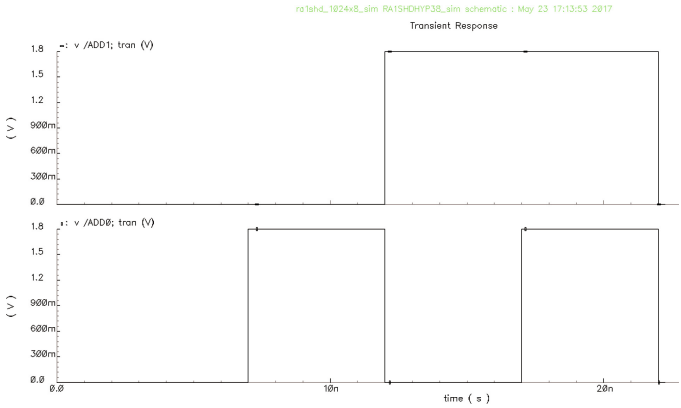

Fig. 5. The input signal excitation for 2–4 decoder transient simulation.

The output signals in simulation experiment are shown in Fig. 6. OUT0–OUT3 is the fore decoding ports of the 2–4 decoder. Since the address input signals are increased gradually from 0 to 3, with a step of 1 and an interval of 5 ns, the OUT0–OUT3 output ports will be high voltage at every 5 ns. These indicate that the address lines are selected.

When the SRAM is in normal mode, the write enable or read enable signal is valid. The corresponding memory cell will write or read data accordingly in each clock cycle. The bit line pairs are controlled, and the bit line data is given by the bit line control circuit in the above process. A bit line control circuit is shown as Fig. 7.

The CS is the selection signal of the bit line, and the GTP is the on-chip clock signal. When the clock is on the rising edge, the GTP rises to the highest voltage, and the bit lines BL and BL_ are pre-charged to the maximum voltage VDD. When the write data enable signal and the bit line signal CS are valid, the bit line BL_ and the BL are controlled by the DW and the DW_ respectively. These determine whether the bit

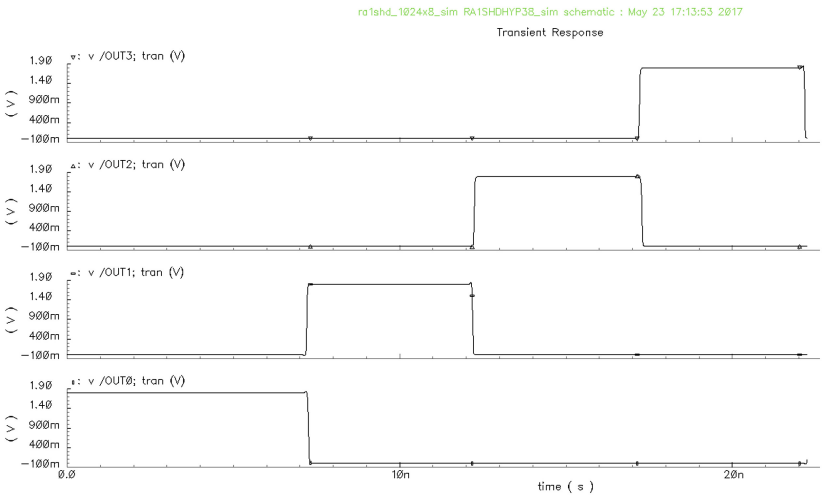

Fig. 6. The simulation output results of 2–4 decoder.

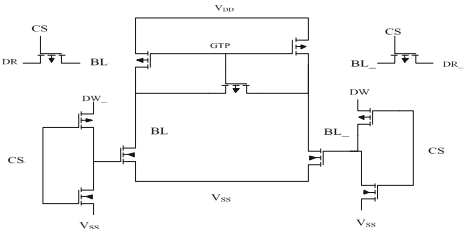

Fig. 7. Bit line control circuit.

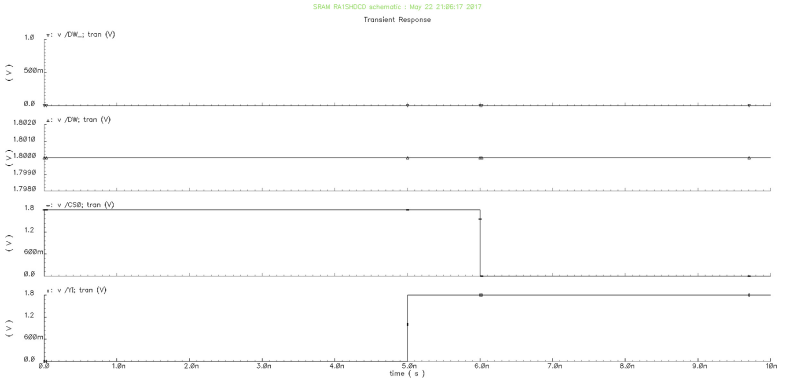

Fig. 8. The transient simulation excitation for bit line control circuit.

lines are pulled down to the low voltage. A voltage difference (VDD-Vss) is formed on a pair of bit lines, i.e., BL and BL_. Data are written successfully into the corresponding memory cell. When the read data enable signal he bit line selection signal CS are valid, the DR and the DR_ are accessed in the bit line BL and the BL_ respectively. The voltage difference signals on the bit line pairs are thus read out.

The input signals used in the simulation are shown in Fig. 8, and the simulation results are shown in Fig. 9.

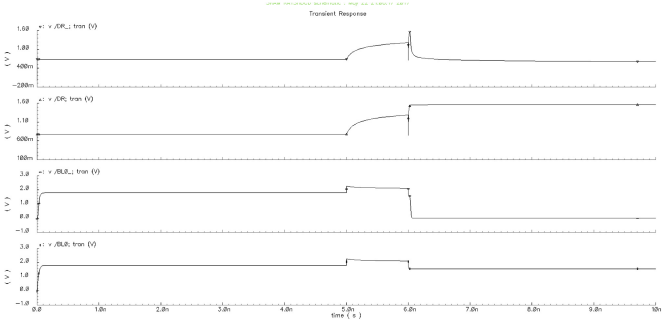

Fig. 9. The simulation results of bit line control circuit.

The bit line charges both the BL0 and the BL0_ to the high voltage because the on-chip clock signal is in a low voltage state at first. The bit line selection signal is so high that the pull-down tubes used to control the bit line pairs are turned off simultaneously. The internal bit line pairs are all at high voltage in the 0–5 ns time periods. The on-chip clock signal is converted to the high voltage in the 5–6 ns time periods. And the bit line selection signal is maintained at a high level. At this time, pull-up transistors and pull-down transistors are turned off, so the pairs of bit lines are in the high impedance. When the on-chip clock signal is maintained at the high voltage, the bit line select signal is converted to the low voltage after 6 ns. At this point, the BL0 and BL0_ signals are controlled by the DW_ and DW for bit lines, respectively. The DW_ signal is the low voltage, and the DW signal is the high voltage. Therefore, the BL0 signal is maintained at a high voltage and the BL0_ signal is pulled down to a low voltage. The data read ports DR and DR_ for bit line are connected to the BL0 and the BL0_ respectively because the bit line selection signal is in the low level. Voltage difference on bit line pair are read out.

When the reading data is simulated for the memory cell, the voltage on the bit line after the pre-charge will change with the voltage on the corresponding storage node. Voltage difference is generated. A sense amplifier is used in the SRAM circuit in order to increase the speed of data reading. When the voltage difference on the bit line reaches a certain value for reading data, the difference is amplified into full voltage through the sense amplifier, so as to improve the speed of data reading. The goal of improving the speed for data reading is achieved. The transient simulation results of a sensitive amplifier are shown in Fig. 10.

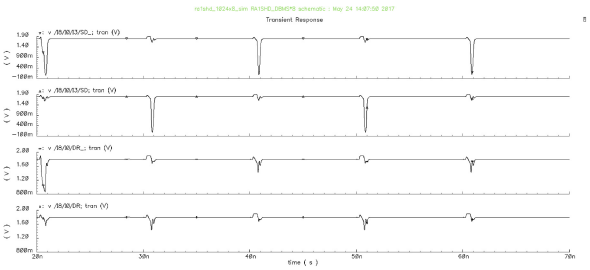

Fig. 10. The simulation results of sensitive amplifiers.

In the simulation results, SD and SD_ are two inverting output ports of the sense amplifier. The DR and DR_ ports correspond to bit lines, BL and BL_ respectively, which signals are read from the memory cell. When the sense amplifier is not in normal operation, the output ports SD and SD_ are pre-charged at the highest voltage. When the voltage difference is generated on the bit line pair, the sense amplifier is excited. At this time, the DR and DR_ ports carry information of bit line pair, thus creating a voltage difference of V_{DR}-$V_{DR\_}$. The voltage difference is detected by the sense amplifier so that the SD or SD_ signal level is pulled down to output the result. The higher the resolution of the sense amplifier, the smaller the voltage difference required for the bit line pair, and the faster the data read in the memory cell, the smaller the power dissipation caused by the bit line voltage swing.

4 The Data Read/Write and Hold Process

In the whole circuit, all of them are effective for low voltage, such as, CEN used as the select signal on chip, OEN as a data read enable signal, WEN as a data write enable signal. The enable signals WEN and OEN are valid in a specified period to control read/write operations by holding CEN on low voltage during the simulation.

In this transient simulation, the funciton of read/write data and hold data are verified by changing the address signal and data signal periodically. The address signals will change periodically over the 00000000-00000001, while the data signal will change over the period of 10101010 and 01010101 during the simulation. The address signals are shown in Fig. 11. The input data signals are shown in Fig. 12.

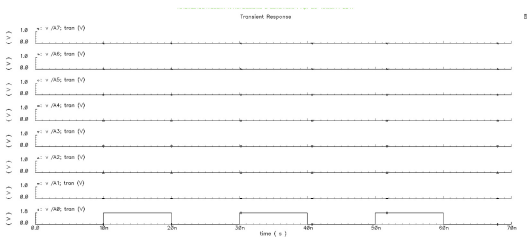

Fig. 11. Address signal.

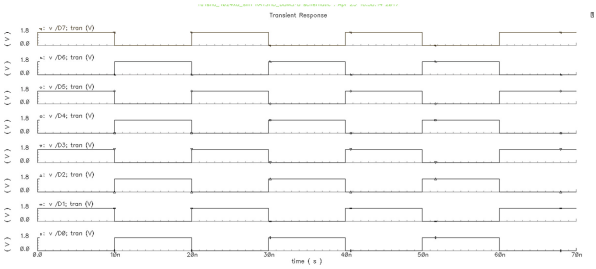

Fig. 12. Data signal.

The period changes of the address signal and the data signal are varied. The control enable signals WEN and OEN are valid within a given time period. The SRAM can be observed to write the two memory cells once respectively. Behavioral level simulation for two data reads are also shown as Fig. 13. Informations can be obtained from the simulation, as follows:

1. The data can be written normally and read correctly for the first time;
2. It can be proved that the read failure is not caused during the first reading process by reading the data correctly second times. The data information can be normally kept in the memory cell under the condition of constant power supply.

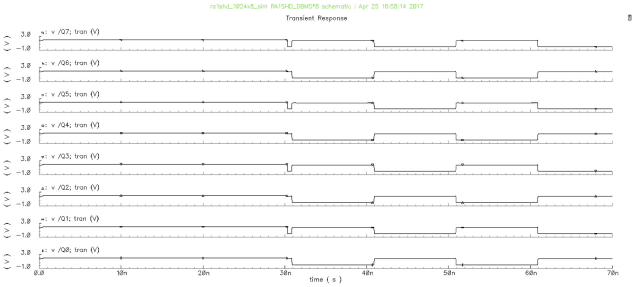

Fig. 13. Simulation for read data.

5 The Randomness for SRAM Circuit

To verify whether SRAM circuit can write or read operations at the same rate for any address cell, eight addresses are selected respectively from 0–255 addresses. As an example, the number information is stored in these addresses and read out. The selected addresses are arranged in order of 0, 5, 80, 90, 120, 50, 180, 250, respectively. The addresses used in the transient simulation are shown in Fig. 14.

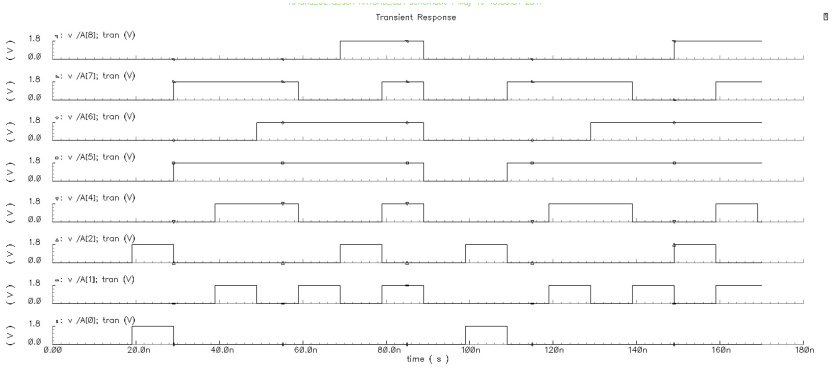

Fig. 14. Address information excitation chart.

The address data will be repeated after 90 ns because the data written needs to be read to verify data consistency. The stored data are shown in Fig. 15.

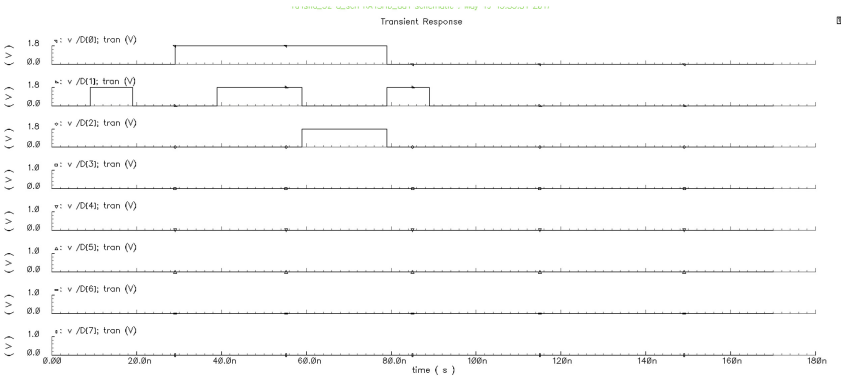

Fig. 15. The stored data signal.

The data is written before 90 ns. The data read operation is performed after the 90 ns according to enable signals. The random write/read function is verified in SRAM.

The transient simulation about 170 ns is completed by applying the address and data information, an external clock signal, and read/write select enable signal, and so on. The read data is consistent with the write data in the simulation results. The data at high 5 bits are kept to zero because each stored data is less than 8. We can only observe low 3 bits data. The comparison results between the write data and read data are shown in Fig. 16.

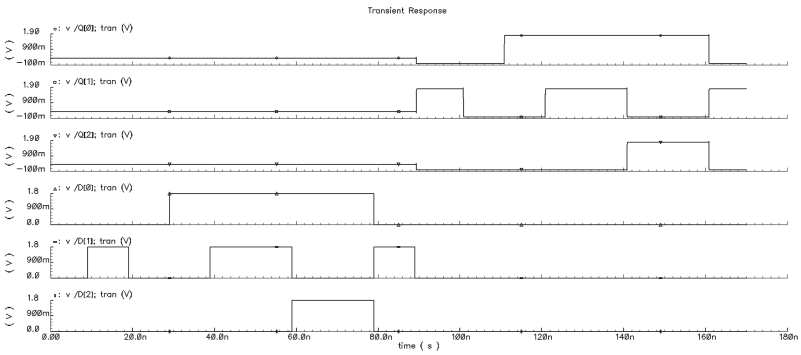

Fig. 16. Compare input data with read data.

D[0]–D [2] is the write data, and Q[0]–Q [2] is the output data in Fig. 16. The output signal remains in the high impedance because the data are written before 90 ns. The signals in output ports are serially output if the data read enable signal is valid. The consistency and randomness of write data and read date can be verified.

The calculation and analysis are carried out respectively in transient simulation, including the data writing process, data reading process and data hold process. The power consumption of writing is 48.33 mw. The power dissipation of reading is 47.83 mw. The power consumes 46.85 mw in the hold process. The operating frequency is 100 MHz.

6 Conclusion

The array based on 6T SRAM memory cell is completed in this paper. The functions of read/write operations and data hold can be achieved in memory array. The peripheral circuits of SRAM are designed and realized, which is decoder circuit, clock circuit and sense amplifier circuit, and so on. The peripheral circuit function can be verified successfully in transient simulation. SRAM function and its read/write randomness can also be implemented correctly.

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