

A Fine Carrier Phase Recovery Method for 32APSK

Yulei Nie^(✉), Zijian Zhang, and Peipei Liu

School of Information and Electronics,
Beijing Institute of Technology, Beijing, China
{nieyulei, 2120150844}@bit.edu.cn, 546641721@qq.com

Abstract. When 32-ary amplitude phase shift keying (32APSK) modulation is used in the communication system, carrier recovery is one of the most important technology. The decision-directed (DD) phase locked loop (PLL) is widely used for carrier recovery. Based on the decision-directed (DD) phase locked loop (PLL) algorithm, the paper proposes a new fine carrier phase recovery method, which is based on the constellation classification and different nonlinear operation. Simulation results show that the performance of the proposed method is much better than the traditional one.

Keywords: Carrier recovery · 32APSK · Constellation classification
PLL

1 Introduction

With the vigorous development of aerospace industry, broadband satellite communications have found wide applications. To settle the scarce problems of available spectrum resources, multi-level modulated signals are utilized to transmit over satellite channels for the improved spectral efficiency. The satellite channel is typically a nonlinear channel, mainly caused by amplifier imperfections. Since the envelopes of the traditional quadrature amplitude modulation (QAM) are not constant, they are very sensitive to channel nonlinearity due to amplitude levels. In contrast to quadrature amplitude modulation (QAM), the amplitude phase shift keying (APSK) is less vulnerable to nonlinear distortions, which is chosen for satellite communications. For example, in the new digital video broadcasting (DVB) standard for satellite communications [3], frequently denoted by DVB-S2, 32-ary amplitude-phase shift keying (32APSK) is recommended as a modulation scheme. However, 32APSK [2] signal is greatly influenced by the frequency offset, which makes the carrier recovery algorithm more complicated.

In digital communication [1], the frequency offset and phase offset are common problems. So the frequency offset and phase offset become key problems in carrier recovery. The frequency offset and phase offset often lead to degradation of communication system performance especially when higher order 32APSK modulation is applied. In order to compensate these two offsets, we have to use the carrier recovery technique. Two methods are often used for carrier recovery. The first method is to directly estimate the carrier information from the received signal. The second method

needs to insert a pilot into the symbol. The carrier information is estimated by the pilot, which is more accurate. The method needs to use frequency estimation algorithm and phase estimation algorithm to eliminate most of the frequency offset and phase offset. In [6–8], the frequency estimation algorithm is introduced in detail. In [9], the phase estimation algorithm is introduced in detail. After the frequency estimation and phase estimation, the PLL is used for carrier recovery. In [3], a hybrid NDA/DD solution has been proposed. This solution performs same nonlinear operation for all the constellation symbols, then seeks the phase error estimation value, which is not accurate. In [4], all the constellation symbols are used. It performs different nonlinear operations on different rings to seek phase error estimation value. Therefore, the phase error estimation value is more accurate. Due to the characteristic of multiple amplitude, the phase error estimation value is affected by the amplitude of symbol, which will cause performance degradation.

To overcome these shortcomings, for the 32APSK fine carrier phase synchronization, we propose a new method. The new method will execute the constellation partitioning for 32APSK constellation firstly, then execute different nonlinear operation for different rings. After these operations, we will use the decision-directed (DD) algorithm to obtain the phase error estimation value which is not affected by the magnitude of the constellation points. For the 32APSK, if the points locate in the innermost ring, they have the smaller radii, and thus their signal-to-additive-plus-adaptation-noise ratio is smaller than the other points [10]. The phase error estimation value will be set to zero.

2 Signal Model and System Structure

Decision-directed PLL (DD-PLL) is a technique used for fine carrier phase synchronization widely. The Fig. 1 shows its structure. It is composed of phase detector, loop filter and NCO (Numerically Controlled Oscillator).

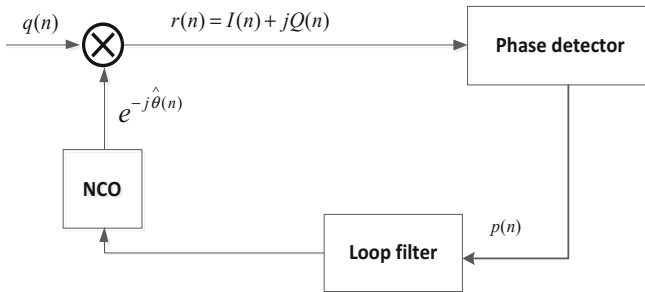


Fig. 1. Structure of carrier recovery loop

As shown in Fig. 1, it is assumed that the channel is an additive white Gaussian noise (AWGN) channel and the input signal $q(n)$ has been subjected to automatic gain control, timing synchronization [5], coarse frequency phase synchronization [6, 7]. The

signal $r(n)$ is generated by using the signal $q(n)$ to multiply the NCO output. Assuming the signal $r(n)$ is written as

$$r(n) = I(n) + jQ(n) \quad (1)$$

The received signal $q(n)$ can be expressed as

$$q(n) = A(n)e^{-j\theta(n)} + v(n) \quad (2)$$

where $A(n)$ is the n -th transmitted complex data symbol, $v(n)$ is white Gaussian noise, $\theta(n)$ is the carrier phase, and it can be written as

$$\theta(n) = \Delta\theta + 2\pi\Delta f n T \quad (3)$$

where $\theta(n)$ is the carrier phase offset, Δf is the carrier frequency offset, and T is the symbol period. The received signal $q(n)$ is multiplied by the output of NCO to produce the phase compensated signal $r(n)$, so the signal $r(n)$ can be written as

$$r(n) = A(n)e^{-j(\theta(n) - \hat{\theta}(n))} + v(n)e^{-j\hat{\theta}(n)} \quad (4)$$

where $\hat{\theta}(n)$ is the estimated carrier phase caused. The phase error is $\theta(n) - \hat{\theta}(n)$, which is obtained by phase detector. The performance of the DD PLL can be improved by solving the output of the phase detector. In general DD PLL algorithm, the phase detector is designed as

$$p(n) = \text{Im}\left[\frac{r(n)}{\hat{r}(n)}\right] = \text{Im}\left[\frac{I(n) + jQ(n)}{\hat{I}(n) + j\hat{Q}(n)}\right] \quad (5)$$

where $\hat{r}(n)$ is the decision symbol of $r(n)$, $I(n)$ is the real part of the $r(n)$, $Q(n)$ is the imaginary part of the $r(n)$, $\hat{I}(n)$ is the real part of the $\hat{r}(n)$, $\hat{Q}(n)$ is the imaginary part of the $\hat{r}(n)$. But the phase error estimate $p(n)$ is affected by energy of signal. To solve this problem, the phase error estimate $p(n)$ can be written as

$$p(n) = \text{angle}(r(n)) - \text{angle}(\hat{r}(n)) \quad (6)$$

where $\text{angle}(x)$ represents the angle of the complex vector x .

For the QPSK signal, the $\hat{r}(n)$ can be written as

$$\hat{r}(n) = \hat{I}(n) + j\hat{Q}(n) = \text{sgn}(I(n)) + j\text{sgn}(Q(n)) \quad (7)$$

where $\text{sgn}(x) = -1$ when $x < 0$ and $\text{sgn}(x) = 1$ when $x \geq 0$.

And the phase error estimate $p(n)$ is computed as

$$p(n) = \tan^{-1}\left(\frac{I(n) * \text{sign}(Q(n)) - Q(n) * \text{sign}(I(n))}{I(n) * \text{sign}(I(n)) + Q(n) * \text{sign}(Q(n))}\right) \quad (8)$$

3 Carrier Recovery Algorithm

The algorithm proposed in this paper is described below. Figure 2 illustrates the normal constellation of 32APSK modulation. According to the figure, we can find that 32APSK constellation has three rings. We assume that r_1 represents the distance between the constellations of the innermost ring to the origin, r_2 represents the distance between the constellations of the middle ring to the origin, r_3 represents the distance between the constellations of the outermost ring to the origin.

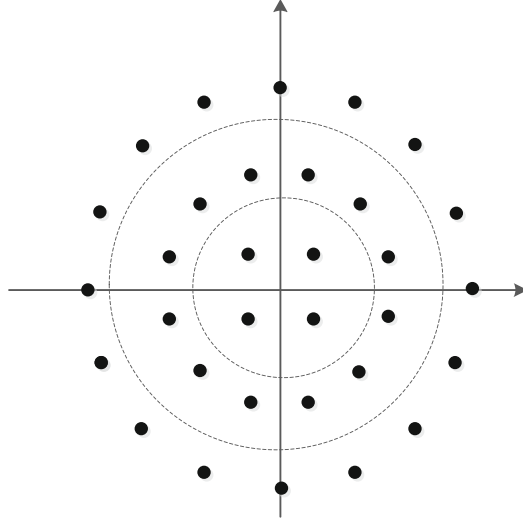


Fig. 2. The constellation of 32APSK modulation

The coordinates for the point of innermost ring can be expressed as

$$r_1 * \exp(j\frac{\pi}{2}k + \frac{\pi}{4})(k = 0, 1, 2, 3) \tag{9}$$

The coordinates for the point of middle ring can be expressed as

$$r_2 * \exp(j\frac{\pi}{6}k + \frac{\pi}{12})(k = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11) \tag{10}$$

The coordinates for the point of outermost ring can be expressed as

$$r_3 * \exp(j\frac{\pi}{8}k)(k = 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15) \tag{11}$$

As shown in Fig. 3, assuming the signal $r(n)$ is written as

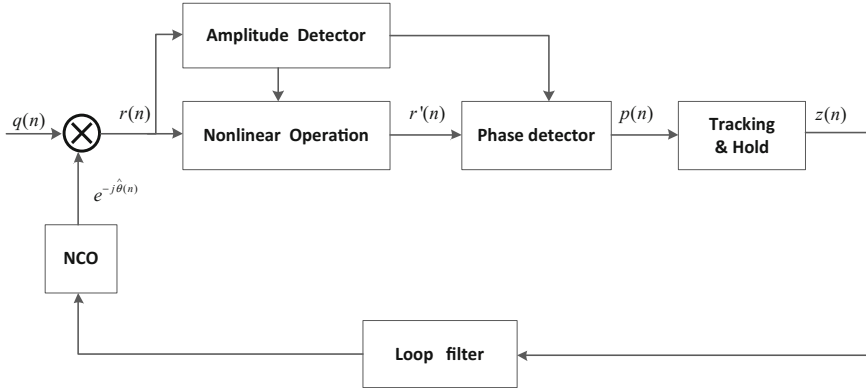


Fig. 3. Carrier recovery loop for 32APSK

$$r(n) = I(n) + jQ(n) \tag{12}$$

When the signal enters the phase-locked loop, firstly it is necessary to decide the position of signal. If the signal is located in the outermost ring, we first use four order operation for the signal and then rotate it with an angle of $\frac{\pi}{4}$, so the transformed signal can be written as

$$r'(n) = (r(n))^4 * \exp(j\frac{\pi}{4}) \tag{13}$$

After the transformation, the constellation on the outermost ring is similar to the QPSK constellation. If the signal is located in the middle ring, we will use three order operation for the signal, so the transformed signal can be written as

$$r'(n) = (r(n))^3 \tag{14}$$

After the transformation, the constellation on the middle ring is similar to the QPSK constellation. If the signal is located in the innermost ring, we will not process the signal. So that the 32APSK constellation is approximately converted into QPSK constellation whose amplitudes are different. Based on the above results, we can reference the QPSK signal to obtain the phase error estimation value.

In the following, we will reference Fig. 3 to introduce the process of obtaining the phase error estimate $p(n)$. After the nonlinear operation for 32APSK constellation. All the rings have become similar to the QPSK constellation. Because the 32APSK modulation is a high order modulation, using the point on the innermost ring to calculate phase error estimate $p(n)$ will increase the phase-locked loop jitter. That will influence the performance of the PLL. So if the point locates in the innermost ring, the phase error estimate $p(n)$ will be set to zero.

3.1 The Amplitude Detector and the Nonlinear Operation

The amplitude detector is used to calculate the amplitude of signal $r(n)$. The amplitude of signal $r(n)$ can be written as $|r(n)|$. Then the signal amplitude $|r(n)|$ is compared to two threshold values τ_1 and τ_2 . According to the size of the $|r(n)|$, we will perform different nonlinear operation for signal $r(n)$. The $r'(n)$ can be calculated as

$$r'(n) = \begin{cases} (r(n))^4 * \exp(j\frac{\pi}{4}) & \text{if } |r(n)| > \tau_1 \\ (r(n))^3 & \text{if } \tau_1 > |r(n)| > \tau_2 \\ r(n) & \text{if } |r(n)| < \tau_2 \end{cases} \quad (15)$$

3.2 Phase Detector and Tracking and Hold

After the nonlinear operation, the signal will be processed by the phase detector (PD). Assuming the signal $r'(n)$ can be written as

$$r'(n) = I'(n) + jQ'(n) \quad (16)$$

The signal $p(n)$ can be written as

$$p(n) = \begin{cases} \tan^{-1} \left(\frac{I'(n) * \text{sign}(Q'(n)) - Q'(n) * \text{sign}(I'(n))}{I'(n) * \text{sign}(I'(n)) + Q'(n) * \text{sign}(Q'(n))} \right) / 4 & \text{if } |r(n)| > \tau_1 \\ \tan^{-1} \left(\frac{I'(n) * \text{sign}(Q'(n)) - Q'(n) * \text{sign}(I'(n))}{I'(n) * \text{sign}(I'(n)) + Q'(n) * \text{sign}(Q'(n))} \right) / 3 & \text{if } \tau_1 > |r(n)| > \tau_2 \\ 0 & \text{if } |r(n)| < \tau_2 \end{cases} \quad (17)$$

The Tracking & Hold output $z(n)$ is defined as

$$z(n) = \begin{cases} p(n) & \text{if } |p(n)| < \alpha \\ 0 & \text{otherwise} \end{cases} \quad (18)$$

4 Performance Analysis

The performance of the algorithm is verified by simulations. In the simulations, we use 32APSK signal, the symbol rate is 1 Mbps. Because the proposed algorithm is used for fine carrier phase synchronization, a frequency estimation algorithm and phase estimation algorithm are adopted to eliminate most of the frequency offset and part of the phase offset. The normalized residue frequency offset is 0.0004. Figure 4 shows the signal constellation diagram before the phase-locked loop. It can be observed signal constellation points are evenly distributed over three rings. However, Fig. 5 displays the signal constellation diagram after the phase-locked loop, discrete signal constellation points can be seen clearly. The bit error rate performance is illustrated in Fig. 6 for comparing with the other two methods. It can be seen that the proposed method has a lower bit error rate in the low SNR region.

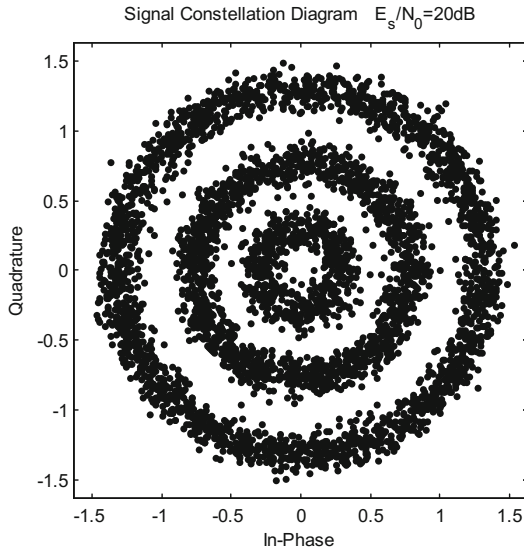


Fig. 4. Signal constellation diagram before the PLL (SNR = 20 dB)

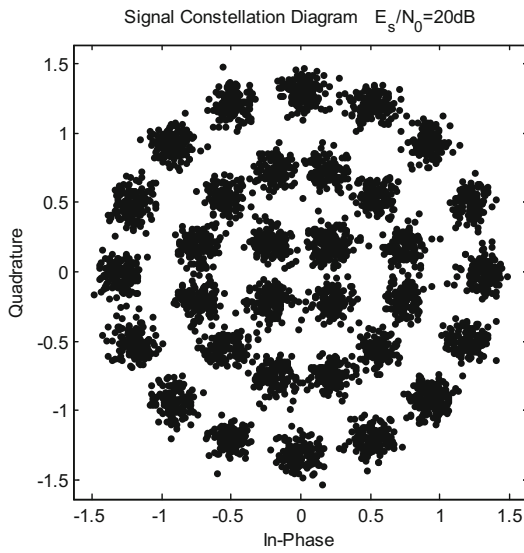


Fig. 5. Signal constellation diagram after the PLL (SNR = 20 dB)

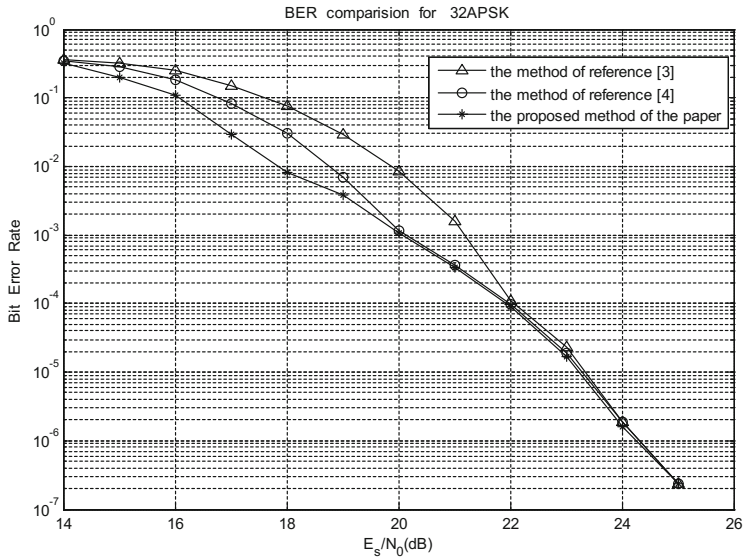


Fig. 6. BER comparison for different algorithms

5 Conclusion

In this paper, an improved decision-directed (DD) algorithm based on the phase-locked loop is proposed, which has a better performance in terms of bit error rate. This performance is especially good in the low SNR region. Compared to the traditional methods for 32APSK signal, the proposed method has better performance. The proposed method can be easily implemented and has a good practical significance.

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