Smart Home Monitoring System Based on SOC

Haiquan Ma, Ping Wang^(⊠), Hong Fan, and Wujun Xu

Engineering Research Center of Digitized Textile and Fashion Technology, College of Information Science and Technology, Ministry of Education, Donghua University, Shanghai 201620, China mahaiquan8@163.com, {PingWang,dhfanhong,WujunXu}@dhu.edu.cn

Abstract. Smart home technologies can provide financial savings, enhance convenience for consumers, contribute to more ecological and sustainable living, and reinforce the buyer's sense of safety and security. The Zynq-7000 AP SoC device is based on the Xilinx® All Programmable SoC architecture. These products integrate a dual core ARM® CortexTM-A9 MPCoreTM based PS and PL in a single device. The PS is equipped with two Gigabit Ethernet Controllers. The goal of this paper is to present a smart home monitoring system, which utilizes face detection as identification. Combining with SOC technology, ZYNQ platform is used to accelerate the speed of video image processing and identification. The system consists of video image acquisition module, control recognition processing module and information display interactive module. With the intelligent analysis, early notice and warning on collected video information informs users via WeChat. The system meets the miniaturization, integration of the home environment at the same time to be more secure and fast real-time information feedback.

Keywords: Smart home \cdot Zynq-7000 AP SoC \cdot Face recognition \cdot WeChat applications \cdot Hardware acceleration

1 Introduction

With the continuous improvement of living standards, people expect home life can be more comfortable, safe and convenient. However, the traditional home applications cannot provide a satisfactory software and hardware conditions to meet these needs. In recent years, collaborative design of software and hardware has made smart home environment possible. Smart home needs provide not only WiFi solutions but also cloud storage and data analysis services. The companies have provided software and hardware solutions that traditional hardware products are now get connected to achieve data sharing for smart home. The Zynq®-7000 family is based on the Xilinx® All Programmable System on Chip (AP SoC) [1] architecture. Zynq-7000 is the first tightly integrated high-performance ARM Cortex-A9 hard core with programmable logic FPGA device. In the Zynq platform, the programmable logic can be regarded as the peripherals of the processor, and the programmable logic can be regarded as the main device of the processor. Through the perfect combination, it can not only play the advantages of running the operating system, but also show the advantage of FPGA to implement the parallel algorithm to accelerate and reconfigure dynamically.

Zynq-7000 series provides FPGA flexibility and scalability, while providing performance and power consumption and ease of use typically associated with ASIC and ASSP. Zynq-7000 SoC AP family of devices enables designers to use industry standard tools from a single platform for cost sensitive and high performance applications. Although each device in the Zynq-7000 series contains the same processing system (PS), programmable logic (PL) and I/O resources differ between devices [2]. Smart home monitoring system based on SOC in this paper also offers possibilities for energy and cost savings, greater home efficiency through automation, as well as improved home security. Smart homes have the potential to provide for consumers' growing expectations of convenience, sustainable living, safety, and security.

The rest of the paper is organized as follows. Section 2 introduces the architecture of ZYNQ 7000 series. Section 3 briefly illustrates face detection algorithm explored in this work. Section 4 shows the architecture of the proposed system on ZYNQ platform using Vivado HLS [3]. The achieved results are discussed in Sect. 5. Conclusions are offered in Sect. 6.

2 Architecture of ZYNQ 7000 Series

Zyng 7000 SoC from Xilinx is a series of chips that FPGA and CPU are built on the same chip, which can achieve rapid interaction in the accelerated program. Field Programmable Gate Array (FPGA) is becoming more and more popular in the field of computer vision. In view of its true parallel architecture, it can potentially speed up image processing to an order of magnitude. In addition to the FPGA design tools, Xilinx also sells a variety of different levels of FPGA and FPGA resources. They also sell a special type of FPGA chip with integrated CPU on the same chip, called Zynq. This type of chip is classified as SoC. Tight integration between PS and PL [4] is ideal for fast interaction between the accelerator and its controlling C program. With support for DDR3 speed memory interface, it allows the FPGA and CPU to share external memory that is usually much bigger than the available internal memory. All chips of the 7000 series use a Dual ARM Cortex-A9 as CPU. The chip used in this paper is called Zynq 7020 (XC7Z020) and is equivalent to the Artix-7 FPGA. Display and control for ARM part and IP core design for FPGA part are executed. Zynq 7020 possesses rich logic resources that are shown in Table 1. In this thesis the Zyng-7020 is used to test systems designed with the Vivado Design Suite, a toolchain of programs which Vivado HLS extends. The Zyng-7020 can be evaluated with the ZC702 Evaluation Kit that contains interfaces for expansion cards and HDMI 5 output among other features. The system uses camera with USB interface to obtain surveillance video for intelligent analysis (Fig. 1).

Parameter	Description	
Processor	Dual-core Cortex-A9 with NEON and FPU	
	extensions	
Maximum processor clock frequency	$866\mathrm{MHz}$	
Programmable logic	Artix-7	
Number of triggers	$866\mathrm{MHz}$	
6 Enter the number of LUTs	53,200	
32 Kb block RAM quantity	140	
Number of DSP48 chips $(18 \times 25 \text{ bits})$	220	
Select IO input/output block number	HR:200 HP:0	

Table 1. Zynq 7020 chip resources.

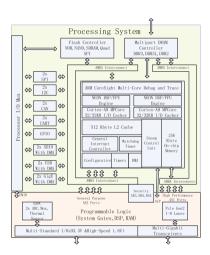


Fig. 1. Zynq-7000 AP SoC overview.

3 Face Detection Algorithm

3.1 AdaBoosting Face Detector

The AdaBoost Algorithm [6] is a kind of creative method for real-time target detection, and its training speed is very slow, but it is very fast. It is an integral image based on fast feature evaluation And the enhancement of feature selection, which is mainly used to quickly reject the attention cascade of non face to face windows.

Boosting is a classification scheme that works by combining weak learners into a more accurate ensemble classifier. A weak learner need only do better than chance.

Training consists of multiple boosting rounds. During each boosting round, we select a weak learner that does well on examples that were hard for the

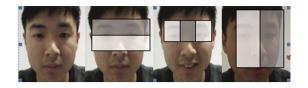


Fig. 2. Image features.

previous weak learner, "Hardness" is captured by weights attached to training examples.

As shown in Fig. 2. The integral image computes a value at each pixel (x, y) that is the sum of the pixel values above and to the left of (x, y), inclusive. This can quickly be computed in one pass through the image.

Each Haar features correspond to a weak classifier, but not any Haar feature can better describe the face's gray distribution for a certain characteristics. How to choose from a large number of Haar features out optimal Haar features and make into classification that used for face detection is the key problem to AdaBoost algorithm training. The AdaBoost Algorithm is mainly implemented by calling the visual library of Open Source Computer Vision (OpenCV). OpenCV is the most popular computer vision library. It is a distributed under the BSD license (open source), cross-platform computer vision library, which can run on Linux, Windows, Mac OS and Android operating systems. It's lightweight and efficient - made up of a series of C function and a small amount of C++ class, at the same time provides the Python, Ruby, MATLAB language interface; realize the many general algorithm of image processing and computer vision. Xilinx provides a C++ library, which can accelerate the similar function of OpenCV. A library is a subset of OpenCV functions and data structures that can be synthesized by Xilinx rewriting.

3.2 KLT Face Recognition Algorithm

Face recognition is a supervised learning process. Intuitive distance was calculated directly, but there is a very big defect - too big amount of calculation. For an image size is 100 * 100, and there are 1000 training set, so the number of calculations required to identify an image is $1000 \times 100 \times 100$. The recognition speed is very slow when the test set is large. A key way to solve the above problem is to dimension reduction of image using Karhunen-Loeve Transform (K LT) [7] by only retaining some key pixel that make recognition speed boost.

KLT transform performs the statistics of the variables in each variable rate of change (the difference between the average of multiple samples and one sample) to achieve dimension reduction, The rate of change is small (the eigenvalue of the covariance matrix is small) that doesn't make much contribution to the discrimination, so it can be discarded; And the variable with large change rate has a great influence on the discrimination, so it is necessary to keep the eigenvector with large eigenvalue to form a transformation matrix. Converting the newly acquired observations and the transposed conversion matrix can reduce the dimension of the original data. This process can be understood as a projection transformation that projects the original high-dimensional spatial coordinates into low-dimensional space. Since the transformation matrix (which is regarded as an orthogonal coordinate axis vector in a low-dimensional space) of the eigenvectors corresponding to several eigenvalues with the greatest contribution has been analyzed before, so this process can maximize the amount of data information is not missing.

The design uses the High-Level Synthesis Tools (HLSTs) which make the system design easier to modify and/or repair to design KLT IP core by Vivado [8]. The Vivado HLS [9] tool convert the C/C++ language to the RTL level HDL description. HLS presents a new design concept, which focus on FPGA design system modeling and improves the development efficiency. HLS Tools allow more software engineers have the opportunity to participate in FPGA design.

4 Architecture of Proposed System

Smart home monitoring system, including the terminal which placed in the user's home and WeChat subscription numbers that users can access through WeChat, two parts. The overall block diagram of the system is shown in Fig. 3.

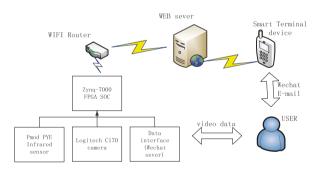


Fig. 3. Home monitoring system data flow.

The PS is equipped with two Gigabit Ethernet Controllers. Each controller can be configured independently. To access pins via MIO, each controller uses an RGMII interface (to save pins). Access to the PL is through the EMIO which provides the GMII interface.

The system uses C170 Logitech network camera to capture video and images, and stored in the wifi router. When a person or an animal to trigger the infrared sensor, the camera is triggered to start recording until the left trigger source monitoring area, the user can view the Home Furnishing by WeChat, and the transfer of view stored in the video server.

4.1 Camera Acquisition Module

C170 Logitech network camera is used to capture video and image, through universal serial bus (Serial Bus Universal, USB) will collect the video storage in SOC memory space. Linux system to carry out video capture, light loaded camera driver is not enough, also need to load V4L (referred to as V4L) module. V4L module supports the programming interface (API) can be applied to call, from the camera device to capture video streaming. The following is mainly about the acquisition of the video stream.

USB is a cable bus that supports data exchange between the host device and a large number of simultaneous access peripherals. Through a host scheduling, token based protocol, the connected devices share the USB bandwidth. When the main device is operating with other peripherals, the USB bus allows you to add, configure, use, and remove peripherals. ZYNQ has two USB controllers, in accordance with the On-The-Go 2 C OTG USB) standard. OTG added to the USB specification, to achieve point to point communication. Using OTG USB technology, consumer electronics, peripherals and portable devices can be connected to each other.

Based on OTG USB, both can be fully compatible with the development of USB peripherals, and can act as a host of USB. Based on the connector signal, the OTG state machine can determine the role of the device. And then, based on the connection mode, the device (host or peripheral) is initialized with the appropriate operation mode. When the device is connected, based on the implementation of the business, the device can use the OTG protocol to confirm its role.

4.2 The PYE Pmod Infrared Sensor Module

According to the requirements of this design, when some people or animals through the surveillance area will trigger the camera video, which requires the appropriate passive pyroelectric infrared sensor module. Combined with the design of the ZYBO development board, the company chose the digilent company's new products are still in the testing phase of the product PYE Pmod infrared human body induction module.

The design of the PYE Pmod infrared sensor module for the German company is still in the test phase of the external expansion.

Exhibition board. It uses a high sensitivity, strong reliability of the original import LHI778 probe, with the BISS0001. The sensor processing integrated circuit is a passive pyroelectric infrared switch. Because of its support in low voltage mode, it is widely used in all kinds of automatic induction and control system. The system uses infrared sensors to a large extent, reduce the power consumption of the system (Fig. 4).

4.3 Smart monitoring system

As shown in Fig. 5, Design system connection diagram including (1) WIFI Router: router network forwarding function; (2) Logitech C170 camera: the camera video

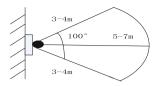


Fig. 4. Pmod PYE infrared sensor.

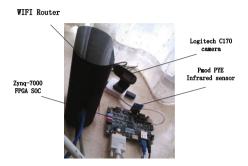


Fig. 5. Design system connection diagram.

data acquisition module; (3) Zynq-7000 FPGA SoC: infrared human body induction module system sleep and video trigger, reduce power consumption; (4) Pmod PYE Infrared sensor: ZYNQ development board as the core control board, including FPGA and ARM two components, data processing and operation display.

The system is open, the main program will enter the state of automatic detection, once someone or animal departure infrared sensor, the main program will be in accordance with the scheduled process or in accordance with the user's configuration to complete all the operations. At this point the user will receive a display home in the case of WeChat subscription number push, and can see the home video online.

WeChat, the leading Chinese mobile messaging app, has released an API for connected hardware that enables users to remote control smart devices through WeChat public accounts. WeChat can be used to send voice, images, and video to a TV, to interact with friends (such as to send reminders and TV "barrages.") WeChat is an information hub that can use its user base and social network relationships to link hardware products, manufacturers, and users, to encourage users to engage with and use hardware products, and to promote sales.

5 Experiments and Results

By using the advantages of the FPGA+ARM architecture of ZYNQ, software algorithm is mapped to hardware implementation. The experimental performance evaluation show that the algorithm can shorten the processing time significantly. Performance comparison between CPUs and SOC for face detection IP core is shown in Table 2.

Experiment	Running time of PC	Running time of SOC
The first experiment	$420.556\mathrm{ms}$	$301.416\mathrm{ms}$
The second experiment	$403.87\mathrm{ms}$	$297.045\mathrm{ms}$
The third experiment	$408.914\mathrm{ms}$	$306.995\mathrm{ms}$

Table 2. Performance comparison between CPUs and SOC for face detection IP core.

It can be found that the average running time is about 300 ms to deal with a face recognition for the hardware algorithm IP. This processing speed relative to the PC on the pure software algorithm reduces the processing time reduces nearly 100 ms, and the hardware implementation of the algorithm achieve a acceleration (Fig. 6).

Diagram of smart home monitoring system is shown in Fig. 7. Infrared camera sensor start the system when someone appear in the monitoring area. The system can accurately analyze the video image, the results are displayed on the platform, including the number of video statistics, matching the face recognition, processing time and receiving message via WeChat, as shown in Fig. 7. The user



Fig. 6. Diagram of smart home monitoring system.



Fig. 7. Receive message screenshots via WeChat.

can view the face image data, also can click the URL to enter the WEB server to view video recording files.

6 Conclusions

In this paper, we show how face detection realizes based on the Zynq-7000 AP SoC device and receive message via WeChat. The system meets the miniaturization, integration of the home environment at the same time to be more secure and fast real-time information feedback. The implementation of face detection and tracking processing using C-based HLS is presented. The results show that hardware accelerators enhance the complex computation of the processing functions. The hardware accelerators on FPGA enhance the computational performance. There are many computer visions application which can take advantage of hardware accelerators to enhance performance of real-time highly computational applications. When targeting HLS design flow, the implementation of C/C++ code is rapidly developed for hardware accelerator.

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