Bit Synchronization and Delayed Decision Feedback Equalization for EDGE BTS - Hardware Implementation on TMS320C6424 TI DSP

Laxmaiah Pulikanti[(✉)], Pradeep Goutam, Bipsa Purushothaman,
K.G. Dileep, and S.V. Hari Prasad

Centre for Development of Telematics,
Electronic City Phase-1, Hosur Road, Bangalore 560100, India
{laxman_p,pradeepg,bipsap,dileepkg,svhari}@cdot.in

Abstract. This paper demonstrates the implementation of bit synchronization and delayed decision feedback equalization for Enhanced Data rates for GSM Evolution (EDGE) system on TMS320C6424 DSP. EDGE makes use of training sequence for channel estimation and inter symbol interference (ISI) cancellation by use of delayed decision feedback equalization. Modulated baseband in-phase (I) and quadrature (Q) signals are generated using Agilent E4438C Vector signal generator and faded using Agilent fading simulator, is used as input to the DSP. Bit Error Rate (BER) performance of uncoded bits for Packet Data Traffic Channel (PDTCH) meets the EDGE standards. Software implementation uses fixed-point C and Integrated Development Environment (IDE) used for development is code composer studio (CCS). Prototyped our design in Texas Instrument TMS320C6424 DSP and verified for all propagation models as per the EDGE standards. The design and hardware implementation of this Demodulator is done for C-DOT indigenous Shared GSM Radio Access Network (SGRAN) Base Transceiver Station (BTS) project.

Keywords: Viterbi equalizer · SGRAN BTS · The design prototyped in DSP · DDFSE · MMSE · DFE · CCS · Centre for Development of Telematics (C-DOT)

1   Introduction

To increase the data transmission rate and to improve network capacity, EDGE was introduced, which uses higher order modulation scheme 8-PSK (phase shift keying) i.e. three bits per RF modulated symbol as opposed to the original one bit per symbol in Global system for mobile communication (GSM). GSM is a digital cellular communications system and one of the most popular personal communication systems which is ubiquitous in the world, especially in Asia. It operates in the 900 MHz and 1800 MHz frequency band, each carrier is spaced 200 kHz and supports eight traffic and data channels per Time division multiple access (TDMA) frame.

The purpose of a detection algorithm is to produce a reliable decision of the input sequence given the received data. With higher modulation scheme used in EDGE, a maximum likelihood sequence equalizer (MLSE), which gives optimum performance,

become unsuitable for cost effective implementation. Since computational complexity of an MLSE increases with channel spread and signal constellation size. Therefore sub optimal technique such as decision feedback equalization followed by reduced state Viterbi algorithm becomes ideal candidate.

In this paper, we present an economical hardware realization of the Delayed decision feedback equalization in EDGE receiver on Texas Instrument (TI) DSP TMS320C6424 [7]. The multipath propagation of a mobile radio channel may lead to a flat fading or frequency selective fading. In the frequency selective fading case, the width of the multipath delay profile exceeds the bit period which results in a time varying ISI spanning over several bits period. To mitigate this ISI a hardware realization of the MMSE DFE [2] followed by reduced state Viterbi algorithm is discussed.

2   EDGE Transmitter

The modulating symbol rate is $1/T = 1625/6$ ksymb/s (i.e. approximately 270.833 ksymb/s), which corresponds to $3 \times (1625/6)$ kbit/s (i.e. 812.5 kbit/s) [5]. T is the symbol period.

The modulating bits are Gray mapped in groups of three to 8-PSK symbols by the rule

$$s_i = e^{j2\pi l/8} \tag{1}$$

Where l is symbol parameter given by Table 1. The 8-PSK symbols are continuously rotated with 3p/8 radians per symbol before pulse shaping. The rotated symbols are defined as

$$\hat{s}_i = s_i \cdot e^{ji3\pi/8} \tag{2}$$

Table 1. Mapping between modulating bits and 8-PSK symbols parameter l

Modulating bits $d_{3i}, d_{3i+1}, d_{3i+2}$	Symbol parameter l
(1,1,1)	0
(0,1,1)	1
(0,1,0)	2
(0,0,0)	3
(0,0,1)	4
(1,0,1)	5
(1,0,0)	6
(1,1,0)	7

These symbols are filtered by linearized Gaussian minimum shift keying (GMSK) pulse. Figure 1 shows the mapping of bits into 8-PSK symbols.
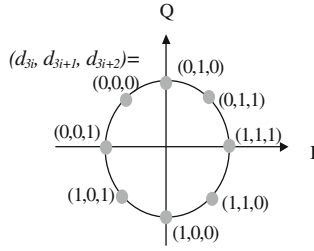
Fig. 1. Symbol mapping of modulating bits into 8-PSK symbol

3   Channel Estimation and Bit Synchronization

The channel estimation and timing synchronization utilize the knowledge of the 78- bit training sequence code (TSC) present in the EDGE burst as in Fig. 2. The channel estimator as in Fig. 3 has the sampled received signal y_k as input. y_k is a sampled sequence which is expected to contain the received EDGE burst. There are eight training sequence codes defined for the normal burst. All the training sequences have good autocorrelation properties.
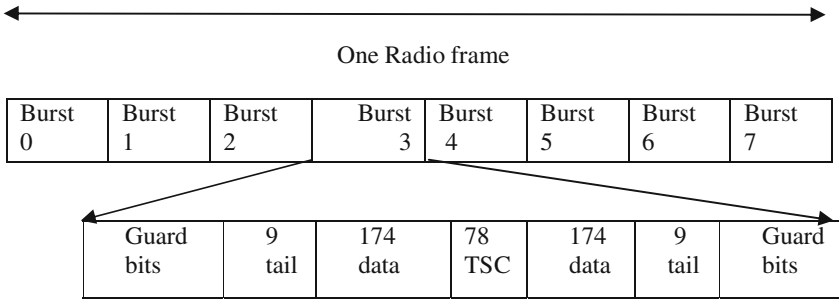

Fig. 2. EDGE Normal burst structure

A sliding window technique is used as in [3, 6] for searching start of the burst. The Eq. (3) represents received signal as $y(t)$, the channel-input data symbols as x_k and the channel-impulse response as $h(t)$; where $n(t)$ is additive white Gaussian noise (AWGN) and T is the symbol duration

$$y(t) = \sum_{m} x_m h(t - mT) + n(t) \tag{3}$$

The channel output as given by (3) is sampled at l times of the symbol rate. By grouping $l = OSR$ (oversampling ratio) successive samples into vectors in the channel out, noise and channel impulse response, we can write the sampled output of the channel as
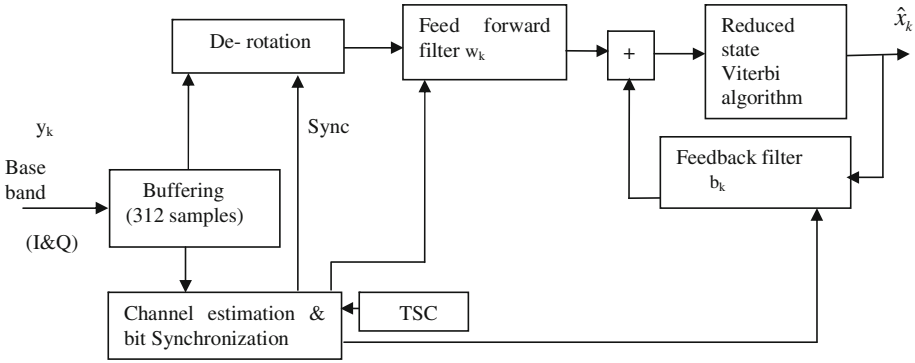
Fig. 3. Functional block diagram of EDGE Receiver

$$y_k = \sum_{m=0}^{\eta} h_m x_{k-m} + n_k \tag{4}$$

Where η is called the channel memory. The first step in the sliding window technique is to convolute received signal y_k with conjugate of known training sequence T_{seq}.

$$p = y_k \otimes T^*_{seq} \tag{5}$$

Here, **p** is an intermediate result, and all samples in **p** are immediately squared to yield an energy estimate **e.**

$$e[n] = p[n]^2 \tag{6}$$

Now the window energy '*we*' is found using as in (7),

$$we[m] = \sum_{k=m}^{m+Len} e[k]^2 \tag{7}$$

Where $Len = \eta \times OSR - 1$. The sample $\mathbf{m_{max}}$ in *we* containing the highest energy value is estimated as directly corresponding to the first sample of the channel impulse response in **p.** From $\mathbf{m_{max}}$ in *we* and the known OSR, it is now possible to extract an estimate of the channel impulse response and also calculate the beginning of the burst. The number of samples in the estimated h is $(\eta + 1) \times OSR$. In the described procedure the entire y_k sequence is processed. In the actual implementation, however, only a sub-sequence is processed. This is possible since the location of the training sequence within an EDGE burst is known.

4   MMSE-DFE Filter Coefficient Calculation

The name MMSE-DFE [2] implies that the DFE coefficients are derived under MMSE criteria. Here b_k and w_k are the feedback and feed forward filter coefficients derived in minimum-mean square-sense, by making the error orthogonal to the received sequence.

The Eq. (4) can be written as follows:

$$
y_k = \begin{bmatrix} y((k+\frac{l-1}{l}T)) \\ . \\ . \\ . \\ y(kT) \end{bmatrix} \equiv \begin{bmatrix} y_{l-1,k} \\ . \\ . \\ . \\ y_{0,k} \end{bmatrix} ; \; h_m = \begin{bmatrix} h((m+\frac{l-1}{l}T)) \\ . \\ . \\ . \\ h(mT) \end{bmatrix} \equiv \begin{bmatrix} h_{l-1,m} \\ . \\ . \\ . \\ h_{0,m} \end{bmatrix} ; \; n_k = \begin{bmatrix} n((k+\frac{l-1}{l}T)) \\ . \\ . \\ . \\ n(kT) \end{bmatrix} \equiv \begin{bmatrix} n_{l-1,k} \\ . \\ . \\ . \\ n_{0,k} \end{bmatrix} ;
$$

By combining N_f (number of feed forward coefficients) output vectors (each containing l samples) together, (4) can be cast in matrix form as follows [2]:

$$
\begin{bmatrix} y_{k+N_f-1} \\ y_{k+N_f-2} \\ . \\ . \\ . \\ y_k \end{bmatrix} = \begin{bmatrix} h_0 h_1 \ldots h_\eta 0 \ldots 0 \\ 0 h_0 h_1 \ldots h_\eta 0 \ldots \\ . \\ . \\ . \\ 0 \ldots 0 h_0 h_1 \ldots h_\eta \end{bmatrix} \begin{bmatrix} x_{k+N_f-1} \\ x_{k+N_f-2} \\ . \\ . \\ . \\ x_{k-\eta} \end{bmatrix} + \begin{bmatrix} n_{k+N_f-1} \\ n_{k+N_f-2} \\ . \\ . \\ . \\ n_k \end{bmatrix}
$$

more compactly

$$
y_{k+N_f-1:k} = H x_{k+N_f-1:k-\eta} + n_{k+N_f-1:k} \tag{8}
$$

the error sequence is given by

$$
err_k = x_k - \sum_{i=0}^{N_f-1} w_{-i}^* y_{k+i} + \sum_{j=1}^{\eta} b_j^* x_{k-j} \tag{9}
$$

where $(.)^*$ denotes the complex-conjugate transpose. Using the orthogonality principle which states that

$$
E\left[err_k \, y_{k+N_{f-1}:k}^* \right] = 0
$$

when the MSE is minimized, we get

$$
b^* R_{xy} = w^* R_{yy} \tag{10}
$$

where R_{xy} is input-output cross correlation matrix and R_{yy} is autocorrelation matrix.

For minimized error the feed forward filter is given by [2]

$$
w_{opt}^* = b_{opt}^* R_{xy} R_{yy}^{-1} \tag{11}
$$

$$w^*_{opt} = \begin{bmatrix} 0 & b^*_{opt} \end{bmatrix} H^* \left(HH^* + (1/SNR')I_{lN_f} \right)^{-1} \tag{12}$$

where $SNR' = SNR/l$.

The following is the "Cholesky" (lower-diagonal-upper) factorization:

$$R \equiv (1/SNR')I_{N_f+\eta} + H^*H = LDL^* \tag{13}$$

By performing the cholesky factorization of Eq. (12) and find the N_f th column of L, that is required to compute the feedback filter. Once the feedback filter is computed, the feed forward filter is calculated using (12).

4.1   Computing the Feedback Filter [2]

Initial Condition (T/2 Spaced case):

$$G_0(D) = G(D) = \begin{bmatrix} \dfrac{1}{\sqrt{SNR'}} & h^*_1(D^*) & h^*_0(D^*) \end{bmatrix}$$

where $SNR' = SNR/2$.

Recursion:

$$\text{For } i = 0, 1 \ldots N_f - 1$$

$$d_i = \left| G_i(0) \right|^2$$

$$l_i(D) = D^i G_i(D) G^*_i(0) d_i^{-1}$$

$$\begin{bmatrix} \alpha_i & \beta_i & \gamma_i \end{bmatrix} = d_i^{-1/2} G_i(0)$$

$$DG_{i+1}(D) = G_i(D) \begin{bmatrix} \alpha_i D & -\beta_i & -\gamma_i \\ \beta^*_i D & (\alpha_i + |\gamma_i|^2/(\alpha_i+1)) & -\beta^*_i \gamma_i/(\alpha_i+1) \\ \gamma^*_i D & -\beta_i \gamma^*_i/(\alpha_i+1) & (\alpha_i + |\beta_i|^2/(\alpha_i+1)) \end{bmatrix}$$

Output:

$$b_{opt}(D) = l_{N_f-1}(D).$$

4.2   Computing the Feed Forward Filter [2]

From (12) the feed forward filter is given by

$$\begin{aligned} w^*_{opt} &= [0 \ldots .010 \ldots 0]L^* \left(H^*H + (1/SNR')I_{N_f+\eta} \right)^{-1} H^* \\ &= d_{N_f-1}^{-1} u^*_{N_f-1} H^* \end{aligned} \tag{14}$$

where $u^*_{N_f-1}$ is the $N_f th$ row of $L^{-1}_{(N_f+\eta)\times(N_f+\eta)}$. Since L is a monic lower triangular matrix, we have

$$w^*_{opt} = d^{-1}_{N_f-1}\left[\ v^*_{N_f-1}\ \ 0_{1\times\eta}\ \right]H^*$$ (15)

where $v^*_{N_f-1}$ is the $N_f th$ row of the inverse of the $N_f \times N_f$ leading sub matrix of L. w^* can be computed efficiently using the following relation [2]:

$$w^*_i = d^{-1}_{N_f-1}\ \sum_{k=0}^{\min(\eta,N_f-1-i)}\ v^*(k+i)h^*_k : i = 0, 1, \ldots N_f - 1$$ (16)

5 DDFSE

The delayed decision feedback sequence estimation (DDFSE) [1] can be regarded as a hybrid between MLSE and DFE. It's like a Viterbi algorithm working on a truncated (at a length μ) channel impulse response and using a DFE on each branch of the trellis subtracting the post cursor ISI caused by samples $x_{k-\mu-1}, x_{k-\mu-2}, \ldots .., x_{k-\eta}$. Where η is the length of the channel and μ can vary between zero and η.

Equation (17) gives the calculation of branch metric, B, where r_k (feed forward filtered and down sampled of y_k) is the observation at time k, x_k is the symbol at time k and b_k is the feedback filter response.

$$B = (r_k - t_k)^2$$ (17)

Where $t_k = \sum_{i=0}^{\mu} b_i x_{k-i} + \tilde{z}_{k-\mu-1}$ and $\tilde{z}_k = \sum_{i=0}^{\eta-\mu-1} b_{i+\mu+1} x_{k-i}$

Description of the Algorithm [1]:

The DDFSE algorithm recursively finds an approximation to the maximum likelihood sequence estimation problem. It is based on a trellis with a reduced number of states. At time $k + 1$, the algorithm stores for each possible state (for first μ taps)

(1) the best path leading to that state,
(2) the metric of that path,
(3) an estimate of the partial state (using $\eta - \mu$ taps).

The recursion step involves the following.

(a) Computing for each (state, next state) pair the sum of the path metric plus the branch metric given by (17). The estimate, $\tilde{z}_{k-\mu-1}$, is obtained from the estimate of the partial state (using $\eta - \mu$ taps).
(b) For each value of (next state) the best (smallest) metric sum is determined and the (state) which gives rise to the best (smallest sum) edge is selected.
(c) For each value of (next state) an estimate of the partial state is made by applying the partial state estimator the (state) chosen in (b). As in the Viterbi algorithm,

the path leading to each (next state) is found by extending the best path determined in (b).

6 Hardware Realization

The hardware realization of the receiver is done on a 10 layer PCB board with combination of Altera Cyclone 3 FPGA as in [8] and fixed-point TI DSP TMS320c6424 processor [7] that runs at 700 MHz as shown Fig. 4.
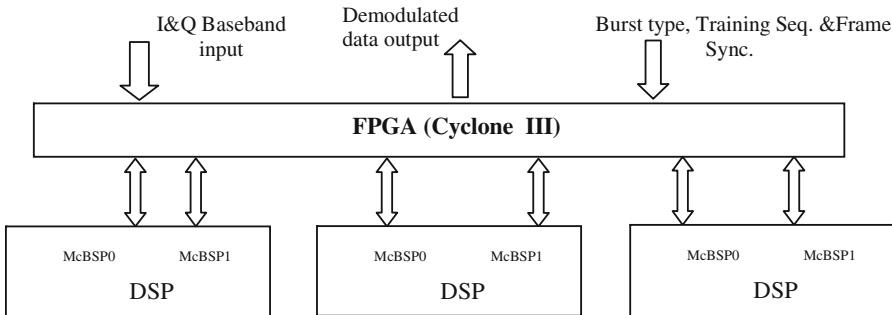

Fig. 4. Hardware realization Architecture

Here FPGA acts as glue logic for interfacing between DSP with other cards of SGRAN BTS. FPGA receives two samples per symbol input data (interleaved I&Q), from down converter (converts RF signal to Baseband). Baseband I and Q samples of 16-bit each is serially buffered to DSP using multi-channel buffered serial port (McBSP) @17.33 MHz.

Received samples are aligned to uplink radio frame (3 times offseted from downlink radio frame) considering all hardware delays in the system using master frame sync of the BTS in DSP. Further DSP performs channel estimation, bit synchronization and DDFSE equalization. Selected parameters for DDFSE are channel memory length (η) of 7 and μ of 1. The total number of 8-PSK modulation symbols is 8 and therefore number of Viterbi states is 8^{μ} i.e. 8 states. The equalized and demodulated data is streamed back to FPGA using same McBSP interface. Currently the system is able to implement two Transceivers (TRX) in one TI C6424 DSP.

The interface rate calculation is as follows:

{[16-bit (I) + 16-bit (Q)] × 2(over-sampling) × 156.25(no. of samples in burst)}/ 0.577 ms (burst period)) = 17.34 Msps. For two TRX, total Bandwidth required:

17.34 × 2 = 34.68 Msps. Each McBSP port of DSP can handle maximum up to 51 Msps. Hence two McBSPs can efficiently handle the required data rate for two TRX.

DSP Resource requirements:

The synchronization and equalization algorithm requires 145 K cycles per burst. So per TRX, the computation required: 145 K × 1733.33 (no. of bursts per sec) = 251.33 M cycles per sec (Mcps). So for two TRX, the computation required: 251.33 × 2 = 502.66 Mcps. DSP can process up to 700 Mcps hence single DSP can easily process synchronization and equalization for two TRX.

7   Performance Analysis and Results

Performance analysis test setup of the system is shown in Fig. 5. The Digital signal interface module (DSIM) receives the uplink EGPRS signal as per the standard from Agilent ESG through PCI card. DSIM digitizes the faded data for different profiles as per settings in Fader Simulator Application on computer as in Fig. 6. The DUT serially receives the digitized I&Q from DSIM and demodulate data bits as explained above sections and feeds back the bits to Agilent ESG.
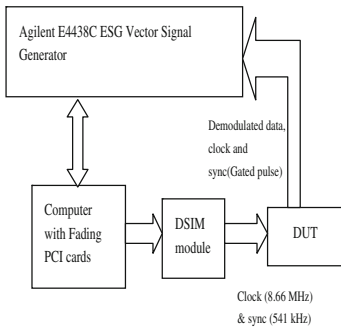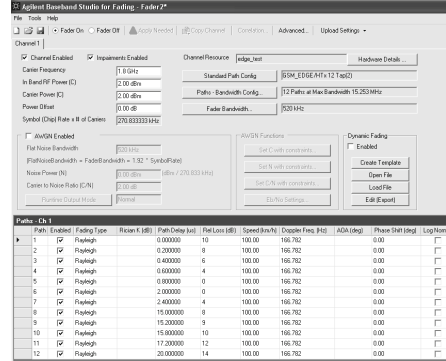

Fig. 5.   Measurement Test setup

Fig. 6.   Agilent fading profiles

The ESG performs the BER measurements on payload PRBS that it has generated for uplink. The BER of the uncoded bits (PDTCH) shall have the limits as in [4] and the measurements for all propagation profiles are given in Table 2.

Table 2.   BER performance

Propagation profile	Specification (PDTCH)	Measured
Static	<2%	0.01780%
RA130(1)	<7%	3.55840%
RA130(2)	<7%	3.84180%
HT100(1) 12 tap	<9%	5.56870%
HT100(1) 6 tap	<9%	3.72750%
HT100(2) 6 tap	<9%	4.86170%
TU50(1) 12 tap	<8%	1.45160%
TU50(2) 12 tap	<8%	1.42030%
TU50(1) 6 tap	<8%	1.92890%
TU50(2) 6 tap	<8%	2.44850%
EQ100	≤3%	2.9250%

Agilent ESG setting:
Frequency = 1.8 GHz, Amplitude = 2 dBm, Payload = PN9, Total bits = 1 Mbits.

8   Conclusions

The implemented demodulator is able to successfully demodulate the data bits meeting the GSM recommendation for all propagation profile as in [4]. Uplink Frame alignment in DSP helps to save significant buffer space requirement in down converter, improving the system design. Viterbi is performed in forward and reverse path from the middle of the burst to reduce the trace back time in trellis. Apart from main DSP which supports two TRX, two more DSP's are added in Architecture for more capacity and flexibility of supporting six TRX. External memory access is not required since code size is less than DSP RAM size of 128 KB. Optimum use of resources in DSP helps to incorporate the implementation of GSM receiver diversity in future.

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