Examination of Power Consumption Reduction and Sampling Behavior of Envelope Detection Based Wake-up-Receiver with Duty Cycling Scheme

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Abstract. In most communication scenarios where the transmission time is short compared to the idle listening time for a data transmission, most power is consumed by the receiver. This brings up the need for a wake-up-receiver (WuRx) embedded in the system. This work presents a WuRx designed out of commercial components in order to investigate the needs of an WuRx embedded in a WPAN in a real environment setup including WLAN and LTE communication and considering interferer rejection. A system design is presented that fulfills all requirements and is designed with regard to enabling a duty cycle scheme for the reduction of the power consumption. Investigation of the duty cycling behavior is shown, technical difficulties are named and the resulting sampling rate and the power saving capability are analyzed.

Keywords: Wake-up-Receiver · WPAN · Duty cycling

1 Investigating a Wake-up-Receiver

Personal area networks, as specified in [1], applications like lightning control, monitoring temperature, moisture etc. or IoT (Internet of Things) devices can demand a fast reaction. If the user activates the light it has to react in milliseconds as we are used to the light switching on instantly. For those applications the receiver has always to listen to the channel. In beacon-enabled networks a fast reaction time can be achieved by a big duty-cycle, resulting in a high beacon number to send and the end devices have to wake up frequently. This results in a high energy consumption. A WuRx designed to support a low data rate modulation can be very simple and consume less energy than a high data rate modulation like BPSK or O-QPSK. In this paper, to gain insight in the switching behavior for an integrated design, a WuRx is used which is build out

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of commercial components on PCB to investigate the needs of a system that includes a WuRx and uses the IEEE802.15.4 transmitter to generate the wake-up frame [2]. Some content of this paper is repeated and summarized from the publication [2] in regard to give a better introduction to the topic. The selection of the components was made with regard to the ability to shut-down, to be able to analyze the behavior when a duty cycle scheme is applied. Challenges will be discussed and solutions presented. In Sect. 2 an overview of the requirements will be given and basics of path loss and link margin calculations are presented. In Sect. 3 the system setup, filter design and resulting link margin is presented. In Sect. 4 the measurements of the WuRx are shown. In Sect. 5 the duty cycling of the wake up receiver is explained and results of measurements are presented which substantiate power savings. Section 6 concludes the paper.

2 Design Requirements

A tuned RF is one of the simplest receiver architectures [3]. It accepts incoming RF signals which are filtered, amplified and converted from RF to baseband by an envelope detector (ED). This eliminates the need for a power consuming local oscillator (LO) completely, which is usually the most power hungry component in a receiver. However, this means that this receiver can only process amplitude modulated signals and the architecture calls for a very high selectivity at RF, which will be explained later in detail. This is a result of the behavior of the ED converting all signals at its input directly to Baseband without selectivity.

The designated transmit distance of our WPAN networks with wake-up receivers is between 5 m and 30 m indoors. In our scenario the wake-up receiver works at the same frequency as the main transceiver. To reduce hardware complexity, the main transceiver will be used to generate the OOK signal. As widely known, a higher carrier frequency enables broader bandwidth and therefore a faster data rate as well as reduced diffraction loss, smaller antenna size and overall increased level of integration. But a higher carrier frequency also increases the path loss and therefore the necessary sensitivity of the receiver. Moreover, additional filtering and amplification at high frequencies is more complex and power hungry. The formula for free space path loss in decibel is:

$$\frac{L_s}{\mathrm{dB}} = 20\ log_{10}\left(\frac{4\pi f d}{c}\right) = 20\ log_{10}(d) + 20\ log_{10}(f) - 147.55 \tag{1}$$

with the carrier wavelength λ[m], the carrier frequency f[Hz], the speed of light c[ms^{-1}] and the link distance d[m]. To calculate the path loss we consider a direct line of sight and no walls and floors, which is equal to a large room. As shown by [4] the path loss exponent then is smaller than 2, so for simplicity we can use the simple path loss equation formula. Hence with a carrier frequency of 2.48 GHz and a link distance of 10 m the path loss would be 70 dB, at 30 m roughly 80 dB. A better insight of indoor wireless coverage can be found in [5]. For WLAN at 2.467 GHz and a distance of 1 m we get $L_s = -40.29$ dB which is a attenuation of 40 dB. Inserting the system specific transmit power P_{TX}[dB] and the ED sensitivity S_{ED}[dB] we can calculate the resulting link margin L_M[dB]. This can be interpreted as the additional gain necessary to be able to detect a signal at the inserted frequency and distance.

$$\frac{L_M}{\text{dB}} = P_{TX} - S_{ED} - 20\ log_{10}(d) - 20\ log_{10}(f) + 147.55 \tag{2}$$

Setting the link margin to zero and solving the equation for d gives the distance at which the signal can be detected.

$$d = 10^{(P_{TX} - S_{ED} - 20\ log_{10}(f) + 147.55)/20} \tag{3}$$

Also considering the overall gain G[dB] and interferer attenuation A_I[dB] of the system and solving the equation for A_I[dB] we can calculate the necessary attenuation for an interferer in a dedicated distance.

$$\frac{A_I}{\text{dB}} = P_{TX} - S_{ED} + G - 20\ log_{10}(d) - 20\ log_{10}(f) + 147.55 \tag{4}$$

For our test system we choose to use the WPAN channel with fewest interferences which is channel 26 at 2.48 GHz. Figure 1 illustrates the down conversion of the RF band to baseband by an ED containing the wake-up signal on WPAN Channel 26 and the two closest interferers, WLAN Channel 13 and LTE Band 7. As shown in the illustration the interferers have potentially higher transmit power than our WPAN node, which has 4 dBm specified as output power of the AT68RF233 transmitter without losses due to the balloon, the antenna or mismatch. As defined in [6] the maximum transmit power for WLAN is 20 dBm and for LTE Band 7 24 dBm as defined in [7]. A narrowband filter in the RF band is necessary to suppress the interferers and only convert down the band of interest. The calculation of the attenuation needed to suppress WLAN signals with transmit power of 20 dBm at a distance of 1 m - for a system using an ED with a sensitivity of −30 dBm - is approximately 10 dB and for LTE with 24 dBm transmit power 13.7 dB, according to Eq. 3.

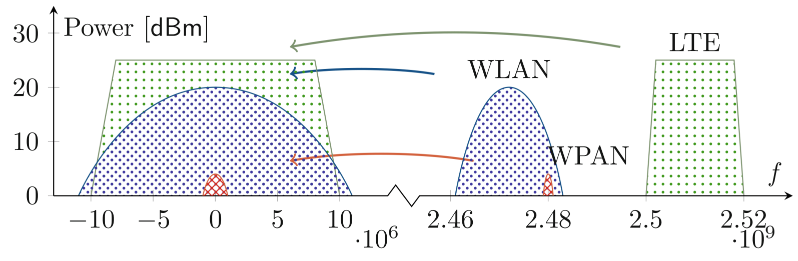

Fig. 1. Down conversion of RF signals to baseband by envelop detection with WLAN and LTE communication as interference

3 System Design

3.1 System Setup

For this work the absolute power consumption of the system is not of interest, since it cannot compete with integrated solutions anyway. The emphasis is on the knowledge gained on how and which parts influence the others. All parts had to be chosen considering manual soldering for fast adaption of changes and debugging.

Figure 2 shows the WuRx with different stages. To achieve a good interferer suppression we designed the WuRx using multiple bulk acoustic wave (BAW) filters with different pass characteristics, which will be explained later. The WuRx sensitivity suffers heavily from the additional attenuation of the bandpass filter configuration. Increased gain is the only way to compensate for the losses, but amplification comes with the cost of power consumption in general.

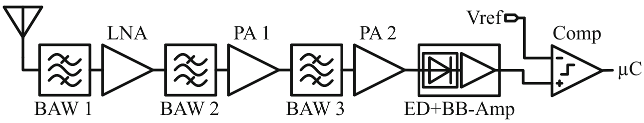

Fig. 2. WuRx system concept with overlapping filters to gain an extremely narrowband filtering

All active components were selected with regard to the switching on/off times and existence of an enable pin. An extraction of some interesting characteristics of the used parts stated in the data sheets are listed in Table 1.

Table 1. Data sheet specifications at 25 °C, 3.3 V, 2.481 GHz

	Current [mA]	Gain [dB]	t_{on} [ns]	t_{off} [ns]
LNA, SKY67159	45.5	17.2	400	150
PA1 + 2, HMC414	494	34	45	45
ED, LTC5508	0.55		8000	
Comparator, MAX9141	0.275		1000	5000
Total	540.3	51.2		

3.2 Narrowband Filter

As mentioned earlier the interferers have higher power than the wake-up signal leading to the necessity of strong suppression. To achieve the necessary interferer rejection we combined multiple BAW filters for different bands which have an overlapping area in the designated frequency range. We chose two BAW filters from Triquint, BAW 885033 ($f_c = 2.442\,\text{MHz}$, BAW3) and BAW 885009 ($f_c = 2.535\,\text{MHz}$, BAW1/2). The resulting combined attenuation at 2.481 GHz is 16 dB, at 2.467 GHz 63.7 dB and at 2.5 GHz 41.5 dB. Thus, the minimum distance to a WLAN transmitter reduces to 0.7 m and to a LTE transmitter to 14.8 m. Adding more attenuation for LTE would add too much attenuation to our signal. With this configuration the system will still be error prone for LTE, but sufficiently robust against WLAN signals.

3.3 Link Margin

The final performance so far presented here, is achieved with simulated data of the architecture and components described before. With a sensitivity of −25 dBm of the ED, a gain of about 35.2 dB of the amplifier and filter stage, we get a sensitivity of −47.83 dBm at 2.481 GHz. With an assumed wake-up signal power of 4 dBm the equation for path loss gives an ideal maximum link distance of around 15.6 m. With the maximum radiation power of 20 dBm and an attenuation of 12.5 dB WLAN signals are rejected sufficiently above a distance of around 0.7 m. Depending on the distance of the base station the radiation power for mobile phones can reach up to 24 dBm as specified in the 3G standard, to which LTE actually belongs (3.9G). The uplink frequencies for LTE go from 2.5 GHz up to 2.57 GHz in Germany. With a total gain of 10 dB for LTE frequencies, these signals overshadow the desired signal significantly, at equal distance to the receiver. A minimum distance of 14.8 m to the LTE transmitter is necessary to not corrupt the wake-up sequence.

4 Implementation and Measurements

Figure 3 shows the measured gain of the system at the output of the last amplifier. With a gain of 26 dB this results in an ideal range of about 3.41 m with a wake-up signal power of 4 dBm. For 2.467 GHz we have an attenuation of 19 dB and for 2.5 GHz a gain of 3 dB. Table 2 shows the resulting current consumption, Gain and on/off times measured for each stage.

Considering optimum matching and operating points of the power amplifiers the general functionality of the circuit was tested. For the output DC voltage of the ED we get a value of about 275 mV for no incoming RF signal. With regard to the input hysteresis and offset of the comparator the threshold is found to be at 284 mV. With a signal generator directly connected to the board, a sensitivity of −20.0 dBm was measured at 2.481 GHz.

Figure 4 shows the PCB. From the SMA connector at the upper left corner the signal path is routed to the lower right corner and ends in an pin header to be connected to a microcontroller board.

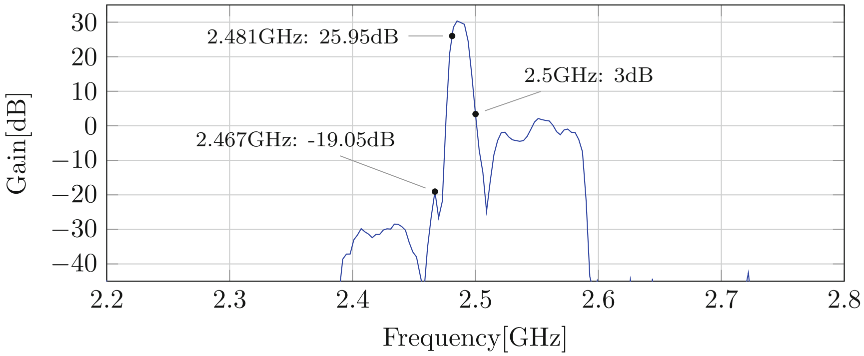

Fig. 3. Measured gain of the complete WuRx

Table 2. Measured electric specifications at 3.3 V supply

	Current mA	Gain dB	t_{on} ns	t_{off} ns
BAW 1+2+3 @2.481 GHz		−16		
LNA	45.5	13.35	397	292
Power Amplifier 1	71.9	12.82	583	371
Power Amplifier 2	73	12.21	772	400
Envelope Detector	0.55		6800	150
Comparator	0.165		3300	5000
Total	191	22.38		

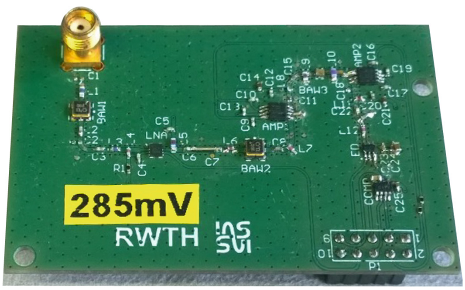

Fig. 4. Wake-up-Receiver PCB

5 Duty Cycling the WuRx

Figure 5 shows the processing of an incoming signal at the input of the first stage. In (a) the incoming wake-up sequence is shown, which is modulated by the transmitter using OOK. The presence of the carrier frequency represents a "1" and the absence a "0". In this example the length of the signal for a bit was chosen to be 200 µs. Therefore, the receiver has a data rate of 5 kb/s. (b) shows the duty cycle for the wake-up-receiver components, that will be switched on and off. One fundamental design aspect of this work is the ability to switch all active components. Thus, the power consumption can be reduced by the factor of the duty cycle, while the receiver is still able to detect a wake-up signal without latency. In this example the on-time was chosen to be 20 µs and the off-time 30 µs, which would decrease power consumption by 60 % The duty cycle has to be adjusted to the used components and the achievable on-off switching times. (c) depicts the filtered and amplified signal and (d) shows the ED output, thus the conversion to DC by the ED. The signal is now nearly reproduced as OOK. The demodulation signal has a low amplitude so it has to be amplified again. Afterwards a comparator converts the signal to an interpretable, digital form. Two different approaches can be taken here. The comparator can be included in the duty-cycle, which decreases power consumption further, leaving the recreation of the wake-up sequence to the following stage, e.g. a logic or microcontroller. This approach is shown in (e). The comparator can also stay on constantly and use its sample-and-hold function to recreate the signal lowering the requirements for the following stage, as shown in (f). At the end of the on-time of the duty-cycle the comparator samples the steady state of the signal and holds it till the next period. As a first value for the sample time 5 µs was chosen, which makes the hold-time of the comparator 45 µs long in this example.

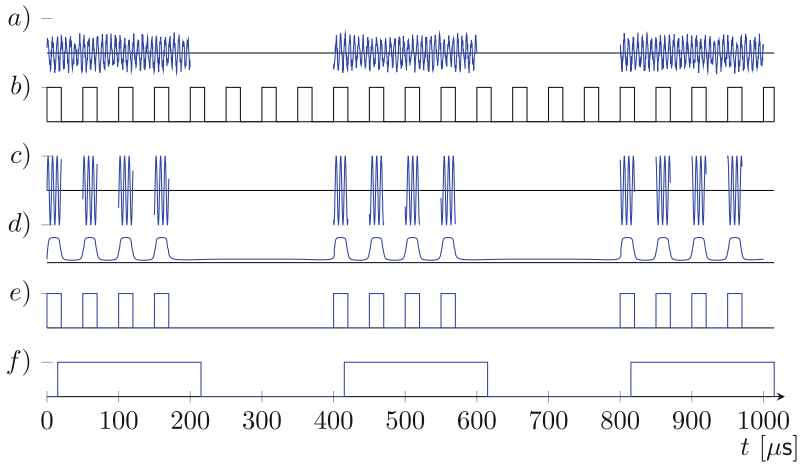

Fig. 5. Sampling wake-up signal with duty cicled WuRx

For the duty cycle all active components were triggered individually, while the rest of the circuit important for the propagation remained constantly on. The signal was measured at the output of the last gain stage, after the ED and after the comparator, to gain insight in influences resulting from the duty cycling. Therefore, a signal generator was connected and adjusted to send a constant signal with a frequency of 2.481 GHz and the output power was set in steps from −47 dBm to −40 dBm to −30 dBm. Additionally, a microcontroller was used to apply the duty cycle to the tested component and served also as trigger source for the oscilloscope. The LNA has an enable time of around 397 ns and a disable time of around 292 ns for all tested output power settings. While the enable time is close to the value given in the data sheet, the disable time is nearly twice as long. For the first power amplifier an enable time of 583 ns and a disable time of 371 ns are measured again for all tested output powers. These values differ heavily from the given 45 ns in the data sheet. Respectively, the second power amplifier has an enable time of 772 ns and a disable time of 400 ns. The ED's measured wake-up time is around 6.8 µs, which is even lower than specified in the data sheet, but still dominates the minimum enable time of the duty cycle. The comparator's enable time is about 3.3 µs, which is again longer than the 1 µs specified in the data sheet and the disable time is around 5 µs.

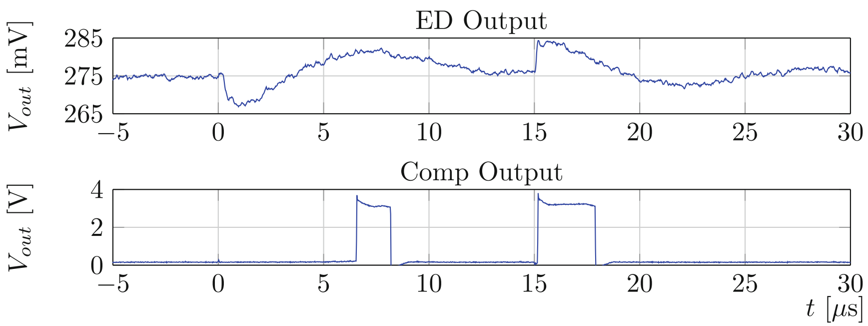

Fig. 6. Swing-in and -out behavior of the circuit

Figure 6 shows the output of the ED when the previous stages are duty cycled. It can be observed that the ED's output drops at 0 µs and than performs a swing in of 12 µs. This causes a wrong detection by the comparator at approx. 7 µs. A second overshoot happens at a falling edge of the duty cycle. The input of the ED had a constant input voltage. This output voltage swing is caused by the power consumption of the amplifier that causes a voltage drop at the ED supply and could not be solved by buffer capacitors. The comparator should be adjusted to sample after the swing-in, stopping shortly before the on-time of the duty cycle, in this setup at 13 µs till 14 µs. Thus it is made sure, that wrong peaks and swing-in behavior caused by the duty cycle have no impact. If the ED is duty-cycled as well, the long wake-up time of about 6.8 µs prevents ringing

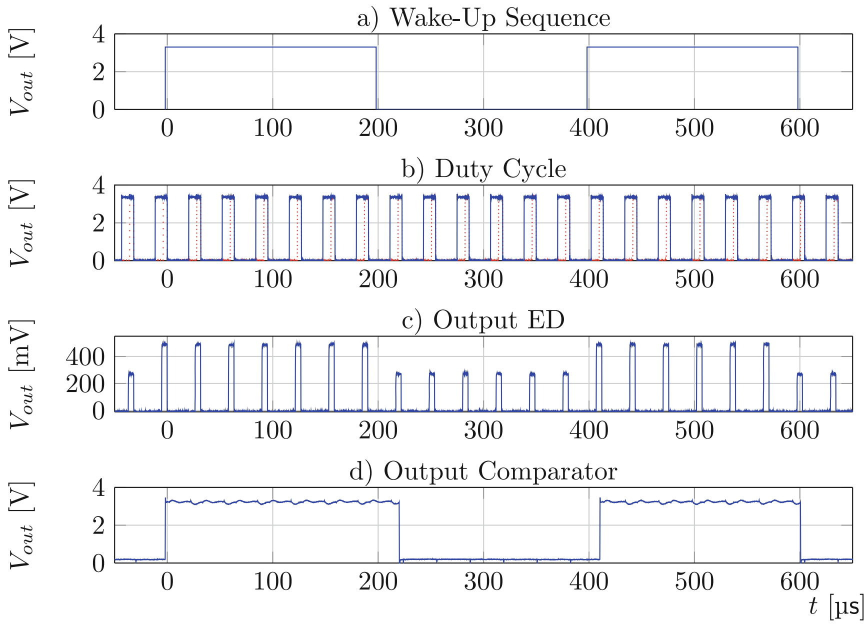

Fig. 7. Sampling wake-up signal with duty cycled WuRx measurement

nearly completely, but for the integrated design which possibly enables a faster activation this should be considered.

Figure 7 shows the measured results of the signal reconstructed by the wake-up receiver. A periodic square wave signal with a length of 200 μs was produced with a signal generator, plot (a). The duty cycle, shown in plot (b), was adjusted to 30 % with an on-time of 12 μs and an off-time of 20 μs. The second trace in b), dotted line, shows the period during which the comparator samples the signal, adjusted here to be in the last microsecond during on-time. Plot (c) shows the output of the ED and plot (d) the output of the comparator, the recovered signal. It is noticeable, that the first pulse is longer than 200 μs by around 24 μs and the second pulse is shorter by about 8 μs. The reason for this is on the one hand the shift between the signal and the sample time of the comparator and on the other hand the period of the duty cycle. The recovered signal will always be a multiple of the duty cycle plus or minus the sample time of the comparator. If the quotient of the bit length of the signal divided by the period of the duty cycle is not an integer, the recovered pulse will therefore vary in length, which has to be considered during detection. The minimum on-time of the circuit to successfully sample the input signal is 8 μs, with a sample time of 0.8 μs. Based on this values different duty cycles can be adjusted and examined, where only the off-time of the circuit is varied and thus the sample rate is changed. To successfully reconstruct the signal pattern with 5 samples at 100 % duty cycle a minimum bit time of 40 μs is needed. To get at least 50 % power saving by the duty cycle scheme the resulting bit length is 80 µs. Changing the bit length to longer time and keep the samples at 5 samples for a bit, which basically means reducing the sample rate, increases the power saving. With a bit length of 1 ms and a sample rate of 5 kHz the resulting duty cycle and power needed is 0.04 % compared to the no duty cycling scheme.

6 Conclusion

In this work we showed the implementation of a WuRx with commercial components to investigate the needs of such a system. It uses discrete off-the-shelf components and was built on a FR4 PCB to have the possibility to measure and analyze the state of the signal after every processing step. Measurements showed a sensitivity of −47 dBm. The WuRx was used to investigate the achievable sampling rate when using a duty cycle scheme. We achieved a maximum on time of 8 µs for one sample and are able to reduce the power consumption to 0.04 % when using a bit time of 1 ms which results in a bitrate of 1 kHz. The behavior of the components working together could be analyzed and lessons from that can be taken into account when integrating a WuRx on silicon.

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