Implementation of a Low-Rate Linear Step FM Transceiver on a Software Defined Radio Platform

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Abstract. Linear FM (Chirp) signals have the merits of constant envelope and insusceptibility to significant carrier frequency offset which particularly suit for low-power low-rate communications. However, the fully digital implementation of the matched filter for the chirp signals is not economically feasible. A low data-rate communication technique using linear step frequency modulated (LSFM) signal was thus proposed which exhibits a complexity reduction in the matched filter implementation with an acceptable performance loss compared to the chirp signals. This paper presents an implementation of such an LSFM transceiver on a realistic commercially available software-defined radio (SDR) platform. Specific system parameters in the LSFM are designed for a furthermore complexity reduction. Implementation cost and experimental results are presented.

Keywords: Chirp communications · Low-rate · Matched-filter · Linear step FM · Transceiver · Software-defined radio

1 Introduction

Wireless communication techniques have been evolving at an exceptional rate recently and will be continually in the near future. Although the mainstream techniques are broadband wireless communications which satisfy the demand of mobile internet services, there are low data-rate techniques due to the growing needs of wireless sensor networks deployment [1]. In a low-rate wireless personal area network (LR-WPAN) standard (IEEE 802.15.4a), the chirp spread-spectrum (CSS) signals are used to support long-range links between sensor nodes.

Chirp signals, also known as linear frequency modulated (LFM) signals, are traditionally used in radar/sonar applications due to its special characteristics in ambiguity function, i.e., pulse compression and Doppler-shift/carrier-frequency-offset (CFO) immunity. Recently the chirp signal has been exploited in communications mainly for immunity against multipath/interference or multiple access purposes [2–8]. The generation of the transmitted chirp signals and the matched filtering in the receiver are mainly relied on the analog surface acoustic wave (SAW) chirped delay lines [9, 10]. In [10], a full-digital implementation of radar chirp pulse compression (matched filtering) using FFT processors is proposed. For a communication system requiring high receiver sensitivity, lower data-rate is mandated and the carrier frequency offset (CFO) between the transmitter and the receiver

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then becomes significant relative to the symbol rate. In this scenario, digital signaling with long symbol period wideband chirps is feasible, which incurs a greater complexity in the digital implementation of the corresponding matched filters. In [11, 12] we have proposed an economic transceiver architecture based on linear step frequency modulated (LSFM) signals, which approximates the chirp signals, and a specific preamble signal designed for symbol/frame/CFO synchronization. The proposed transceiver technique is adequate for physical layer implementation for Low–Power, Wide-Area Networks [13].

This paper presents an implementation of the proposed transceiver on a realistic software-defined radio (SDR) platform which comprises of an RF TX/RX module for RF/Baseband signal conversion and an FPGA for real-time digital signal processing. Implementation cost and experiment results regarding to the receiver performance are given for a specific LSFM system parameters.

2 Chirp Binary Orthogonal Keying with Linear Step FM Signals

In a digital communication system with chirp binary orthogonal keying (BOK), up-chirp and down-chirp signals are typically used to transmit binary data correspondingly. The system model of a chirp BOK communication system with RF frontend and digital modulator/demodulator is shown in Fig. 1. The transmitted baseband signal formulated by

$$s_B(t) = \sum_k s_{a_k}\left(t - k \cdot T_{sym}\right) \tag{1}$$

where $s_{a_k}(t) = \begin{cases} s_{up-chirp}(t), & a_k = 1 \\ s_{down-chirp}(t) = s^*_{up-chirp}(t), & a_k = 0 \end{cases}$, a_k denotes the kth binary data and T_{sym} is the symbol period. A chirp BOK communication system based on a linear step FM (LSFM) signal is proposed in [11, 12] for simplified the digital matched filter implementation, where the traditional up-chirp (LFM) signal $s_{LFM}(t) = \begin{cases} e^{j\cdot\frac{2\pi}{T_{sym}}\cdot\Delta f\left(t^2 - \frac{T_{sym}}{2}\cdot t\right)}, & 0 \le t < T_{sym} \\ 0, & otherwise \end{cases}$, with Δf denoting the frequency swift range $(-0.5\Delta f \sim 0.5\Delta f)$ (chirp span) during the chirp/symbol period T_{sym}, is replaced with

$$\begin{aligned} s_{LSFM}(t) &= \sum_{m=0}^{M-1} s^m_{LSFM}\left(t - m \cdot \frac{T_{sym}}{M}\right), \\ s^m_{LSFM}(t) &= \begin{cases} e^{j\cdot(2\pi\cdot f_m\cdot t + \theta_m)}, & 0 \le t < \frac{T_{sym}}{M} \\ 0, & otherwise \end{cases} \end{aligned} \tag{2}$$

where M $(m = 0 \sim M-1)$, $f_\Delta = \Delta f/(M-1)$ and $f_m = -\Delta f/2 + m \cdot f_\Delta$ denote the number of steps, the frequency step and the instantaneous frequency at the mth step, respectively, while $\theta_m = \theta_0 + \sum_{l=0}^{m-1} f_l \cdot T_{sym}/M$ is the phase adjustment for making the signal continual in phase.

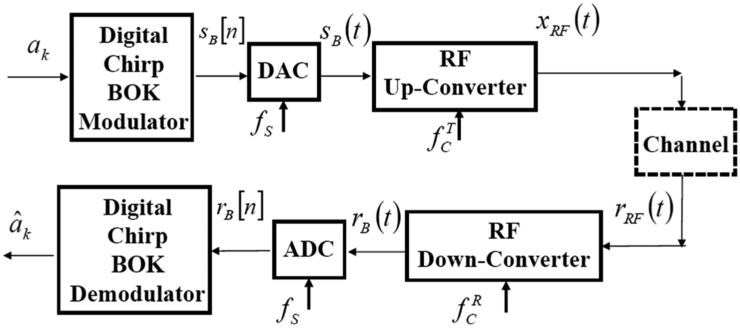

Fig. 1. The system model of a chirp BOK communication system

3 LSFM Transceiver Architecture

3.1 LSFM Transmitter

Figure 2 shows the hardware architecture of the digital chirp BOK modulator (in Fig. 1) with LSFM signals, where $\Delta\omega = 2\pi \cdot \Delta f/f_S$ and $\omega_\Delta = \Delta\omega/(M-1)$ denote the chirp span and frequency step in digital domain with a sampling frequency $f_S = N/T_{sym}$ and $N = M \cdot N_M$. The frame structure is designed with a specific preamble, i.e., 10101010, which facilitates frame/symbol timing synchronization in a scenario with signification CFO, followed by a payload data stream of ***P*** bits length. The main cost of the hardware

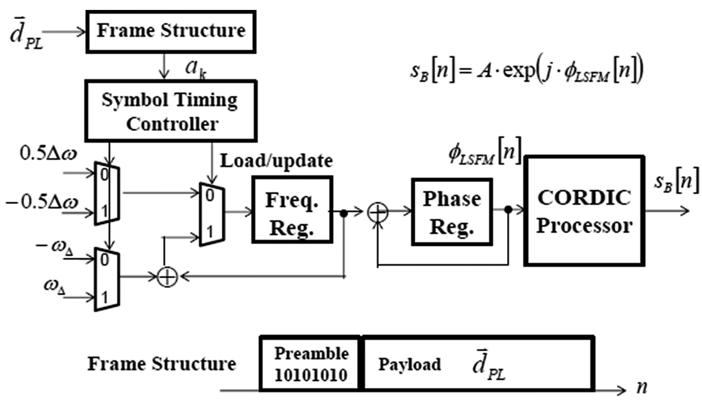

Fig. 2. Digital chirp BOK modulator with LSFM signals

implementation of the digital baseband modulator is thus the phase rotation which can be typically implemented by a CORDIC processor.

3.2 LSFM Receiver

Figure 3 shows the hardware architecture of the digital chirp BOK demodulator (in Fig. 1) with LSFM signals, where $r_M^{down/up}[n]$ denote the outputs of up/down-chirp matched filter depicted in Fig. 4 [12]. Since the transmission is in burst and CFO will cause an offset at the maximum timing of up/down-chirp matched filter outputs, the function of the preamble-based timing synchronizer is to detect start of frame (SOF) transmission and find the adequate sampling timing for the up/down-chirp matched filter outputs. The concept of the preamble-based SOF/symbol timing synchronizer illustrated in Fig. 5 [12]. Having obtained the estimates of the corresponding up/down-chirp matched filter timing based on the particular preamble, i.e., $\hat{n}_{\max}^{up}$ and $\hat{n}_{\max}^{down}$, given by

$$\hat{n}_{\max}^{up/down} = \arg\max_{n} \sum_{p=0}^{N_p-1} \left| r_M^{up/down}[n - 2 \cdot p \cdot N] \right|^2 \tag{3}$$

the payload data is then detected by the following formula

$$\hat{a}_k = \left| r_M^{up}[\hat{n}_{\max}^{up} + k \cdot N] \right|^2 > \left| r_M^{down}[\hat{n}_{\max}^{down} + k \cdot N] \right|^2 \tag{4}$$

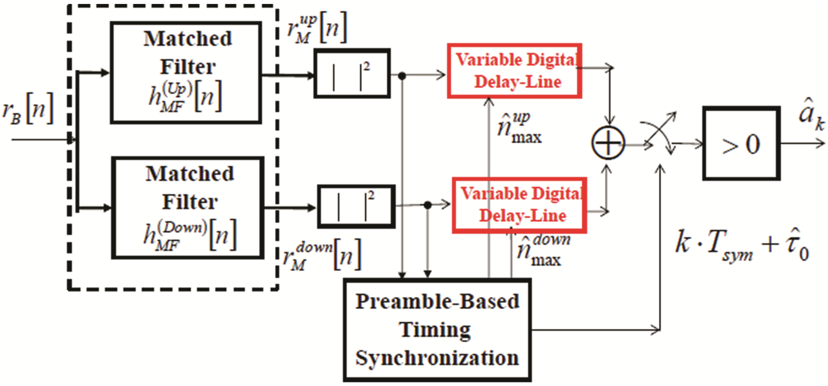

Fig. 3. Digital chirp BOK demodulator with LSFM signals

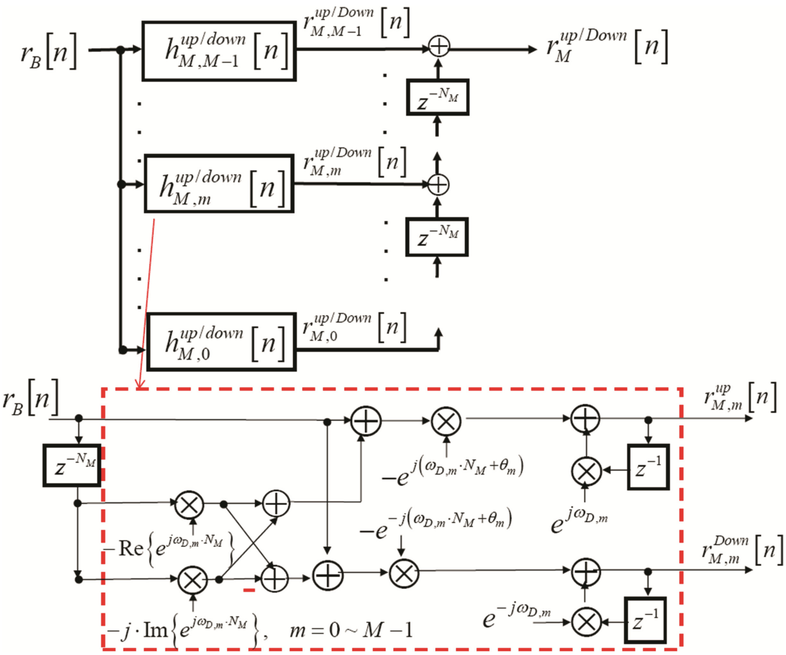

Fig. 4. Low-complexity digital matched filter for up/down-chirp LSFM signals

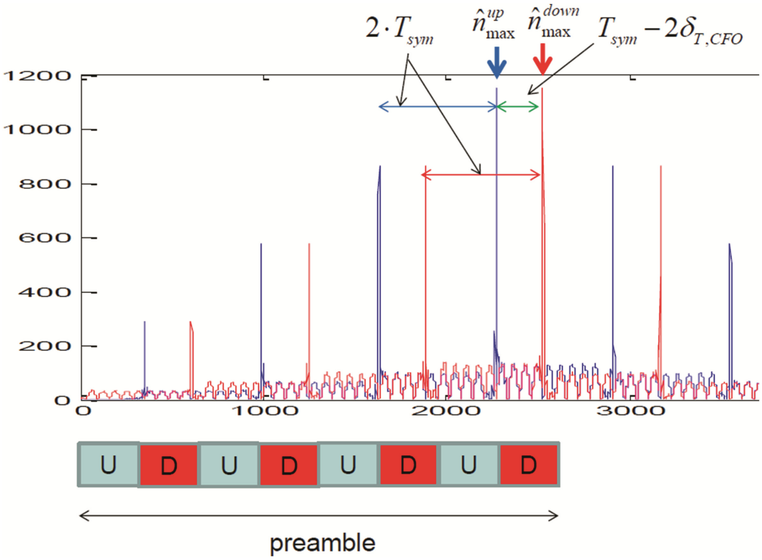

Fig. 5. Illustration of the preamble-based SOF/symbol timing synchronizer

4 Implementation and Experiment Results

The software-defined radio platform used for the implementation of the proposed digital chirp BOK transceiver with LSFM signals is shown in Fig. 6, which comprises the AD9361 EVM as the RF module [14] and the Xilinx/SMIMS AC701 FPGA Evaluation Board as the configurable baseband signal processing module. The specification of the implemented LSFM signals is given as follows: the carrier frequency $f_C = 3$ GHz, the baseband sampling frequency $f_S = 30.72$ MHz, the RF bandwidth $B = 20$ MHz, the chirp span $\Delta f = f_S/4 = 7.68$ MHz, the number of frequency steps $M = 33$, the number of samples per frequency step $N_M = 64$ symbol period which corresponds to $N = M \cdot N_M = 2112$ and the symbol (bit) rate $f_{sym} = f_S/N = 14.5$ Ksymbols/sec. With this specification, the complexity of the matched filter is further reduced since $\exp\left(j\omega_{D,m} \cdot N_M\right) \in \{\pm 1\}$ and $\theta_m \in \{0, \pi\}$, where $\omega_{D,m} = 2\pi \cdot f_m/f_S$ denotes the digital frequency at the mth frequency step. The hardware implementation costs of the digital chirp modulator and demodulator are listed in Table 1. Figure 7 shows the real experimental results of the transceiver with received signal power P_R of -88 dBm, -108 dBm and -118 dBm, respectively. For the $P_R = -88$ dBm case, which is calibrated with a transmission scenario of transmission attenuation 60 dB and $E\left\{\left|s_B[n]\right|^2\right\} = (1800)^2$, the signal spectrum is noticed to rise up from the noise floor. For cases of $P_R = -108$ dBm and -118 dBm, which is achieved by setting the transmission attenuation to the maximum of 70 dB and additional attenuation in digital signal domain with $E\left\{\left|s_B[n]\right|^2\right\} = (1800)^2/10$ and $E\left\{\left|s_B[n]\right|^2\right\} = (1800)^2/100$, respectively, the signal spectrum is submerged in the noise spectrum. The noise power spectral density of the receiver chain in the AD9361 EVM is thus measured to be $N_0 \approx -170$ dBm/Hz. For the cases of $P_R = -88$ dBm and -108 dBm, which corresponds to $E_b/N_0 = P_{R,\min} \cdot T_{sym}/N_0 \approx 40$ dB and 20 dB, respectively, no bit detection error is found in the transceiver experiments. While for the cases of $P_R = -118$ dBm, which corresponds to $E_b/N_0 = P_{R,\min} \cdot T_{sym}/N_0 \approx 10$ dB, a bit detection error rate is found to be $\approx 10^{-2}$. With the maximum TX power of AD9361 known to be $P_{T,\max} = 4$ dBm, the realistic transceiver thus has a margin of channel loss around 122 dB with $P_b = 10^{-2}$.

Table 1. Hardware costs of the implemented digital chirp BOK modem with LSFM signal.

XC7A200T	Slices	DSP48E	RAMB18E
Modulator	943	0	0
Demodulator	1274	160	65

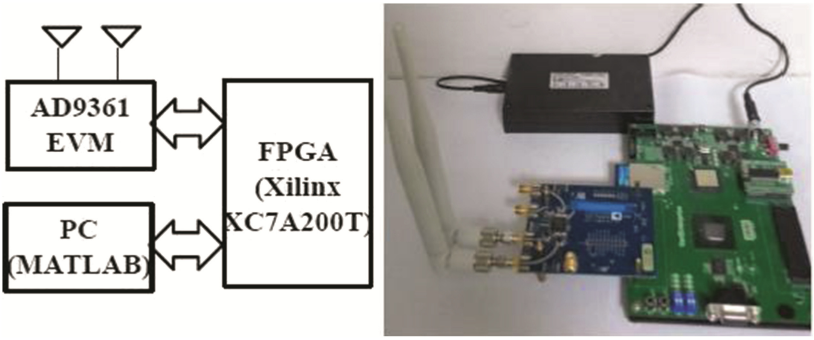

Fig. 6. Software defined radio platform with AD9361 EVM and Xilinx/SMIMS AC701 evaluation board

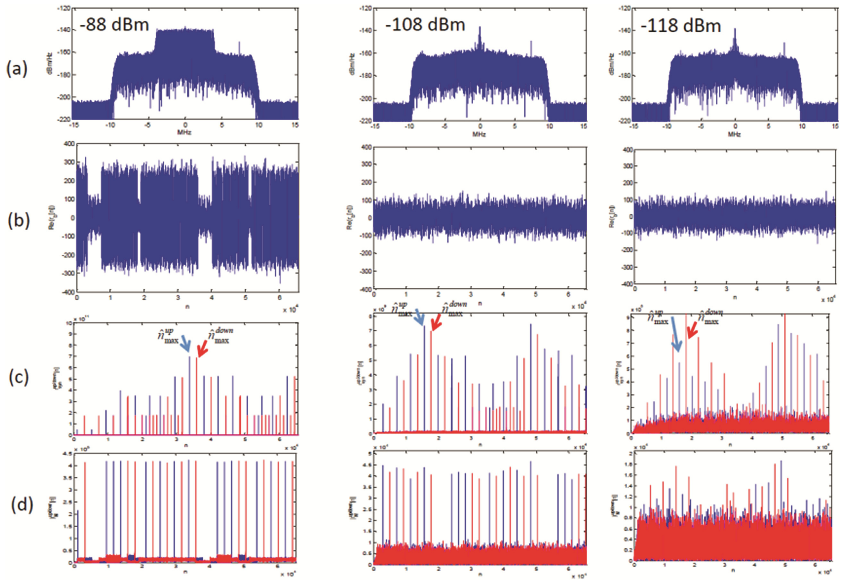

Fig. 7. Experimental results with received signal power of −88/−108/−118 dBm (a) signal power spectrum; (b) real part of received baseband signal; (c) start-of-frame synchronizer output; (d) BOK matched filter output

5 Conclusions

A low data-rate chirp BOK communication technique based on linear step frequency modulated (LSFM) signals exhibits a merit in the matched filter implementation with an acceptable performance loss compared to the traditional chirp signals. In this paper, we present an implementation of such an LSFM transceiver on a realistic commercially available software-defined radio (SDR) platform. Specific system parameters in the

LSFM are designed for a furthermore complexity reduction. The implemented transceiver demonstrates a low-rate wireless data communications which can sustains a margin of channel loss around 120 dB with a bit-error rate lower than 10^{-2}.

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