A 15.5 W Si-LDMOS Balanced Power Amplifier with 53% Ultimate PAE for High Speed LTE

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Abstract. In this paper, a 15.5 W Si-LDMOS balanced power amplifier (PA) technique operating in the 2.620–2.690 GHz frequency band for LTE systems is presented. The amplifier was designed using large signal Si-LDMOS models, which demonstrated saturation P1dB of 41 dBm and 53% PAE. The AM-AM and AM-PM measured data of the balanced amplifier is extracted and embedded in the device under test (DUT) based on IEEE 802.16 OFDM WLAN Transceiver system. A simple linear model was design for behavioral modelling of memory-less baseband digital pre-distorter. The nonlinearity of the balanced amplifier has been compensated using the Simulink version R2011a.

Keywords: Balanced power amplifier (BPA) · Linearity · Power added efficiency (PAE) · Long term evolution (LTE) · Digital pre-distortion (DPD)

1 Introduction

A number of modern wireless communication systems, adopt highly-efficient modulation schemes to enhance spectral efficiency and increase multiple spectral user channels for a wide range of data and voice services. These include orthogonal frequency division multiplexing (OFDM) transceiver systems, such as long term evolution (LTE), wide-band code division multiple access (WCDMA), IEEE 802.16 OFDM WLAN transceiver system and numerous IEEE wireless communication systems [1, 2]. These systems are highly sensitive to nonlinear distortion effects in the transmission path, due to their non-constant envelope. Such systems produce high peak-to-average-power-ratio (PAPR). Subsequently, the source of the nonlinear distortion effects in the transceiver configuration is the RF power amplifier; this research focuses on the design and modelling of a high energy-efficient power amplifier with high linearity [1–3].

The RF power amplifier is an important device not only in wireless communication systems, but also in TV transmission, radar systems and RF heating. The amplitude of radio frequency signal is increase to a certain level of amplification [4, 5]. Spectral efficiency and linearity are the main elements driving the design of power amplifier. The most challenging aspect of power amplifier concept is achieving an excellent efficiency with linearity [6]. However, the design of a power amplifier has to be accomplished in accordance with the system specifications, such as operating frequency, bandwidth, output power, gain, linearity, efficiency and return loss [7]. According to [8, 9], linearity

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is required to sustain information for error free transmission. Efficiency reduces power consumption and improves battery life span at the mobile terminal [5, 10].

The effect of spectral regrowth in power amplifiers has become a major concern in communication systems engineering [11]. Spectral regrowth is the result of non-linearity in the transmission path and leads to in-band and adjacent channel interference [3]. To reduce the effect of nonlinearity and achieve a state-of-the-art system, the power amplifier must be designed carefully to give high data rate and spectral efficiency for high speed broadband services. The best of these technologies embrace higher data rate and higher spectral efficiency from 20 MHz signal bandwidth, downlink data rate of 100 Mbps, with the uplink rate of 50 Mbps obtainable [5, 12] (Fig. 1).

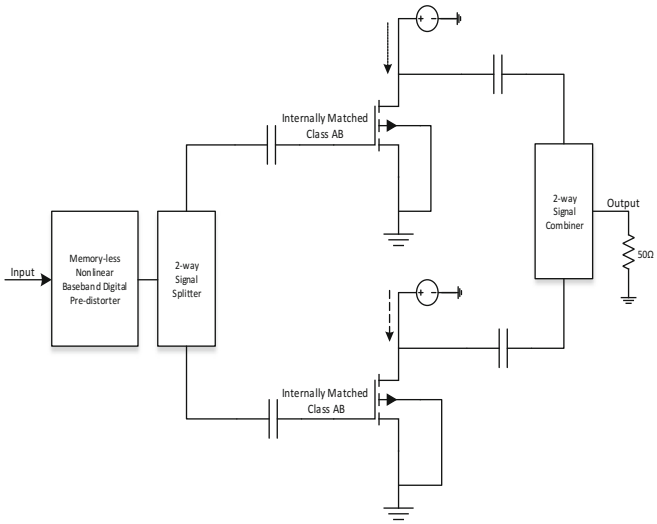

Fig. 1. Balanced power amplifier architecture.

This work is an extension of author's previous work [3] where a design of balanced RF power amplifier is discussed. The amplitude-to-amplitude and amplitude-to-phase characteristics (AM-AM/AM-PM) of the amplifier is used in the modelling of nonlinearities for a wireless metropolitan area network IEEE 802.16 OFDM transceiver. Simulink version R2011a configuration is introduced. Section 2 presents a balanced PA configuration; results will be discussed in Sect. 3. This section also covers the extraction and modelling of AM-AM and AM-PM polynomials in the pre-distorter. Conclusions from the work are drawn in Sect. 4.

2 Balanced Amplifier Design

A balanced power amplifier has been demonstrated in this paper and designed using two transistor models for high data rate, providing efficiency with dynamic range of linearity. Dynamic load adaptation is conveyed by the use of a 50 Ω, quarter wavelength

transmission line impedance inverter. In the design of the balanced power amplifier, there are stages that must be followed to achieve high level performance [13, 14]. The first stage of the design is DC circuit design and simulation. Simulation of the DC circuit determines the bias point and bias network. This is according to the class of operation and power requirement. The bias condition set drain source voltage Vds = 28 V, drain source current (Ids) = 422 mA and gate source voltage Vgs = 2.7 V. The bias network is however designed based on class-AB carrier. The DC simulation results specify the class of operation. The main purpose of good biasing is to prevent signal reflection. The DC quiescent current is obtained to prevent signal distortion [5]. The radio frequency is prevented from going back to the DC source. For the matching network, this transistor requires no matching process, as indicated in the data sheet of the component, input and output impedance are internally matched. The 21 mm length of micro-strip line are connected using line-calc from Agilent advanced design system simulator (ADS) with RT 5880 substrates, parameters; $\varepsilon_r = 2.2$, H = 0.508 mm, z_o = ohms, T = 3 μm and tan $\delta = 0.017$. The 50 Ω line impedance of open and short circuit is incorporated to right angle of the RF blocking transmission lines. A class-AB power amplifier element values have been positioned using tune tool of the ADS simulator for best performance of the proposed system.

Linear and nonlinear simulation was performed for class-AB design. The design and simulation process for a class-AB amplifier is necessary in order to prepare the single stage class-AB design into a multiple stage balanced power amplifier. The linear simulation shows a good flat gain, where the S21 is almost 14 dB, the return loss, S11 and S22 are also good. The nonlinear single tone simulation result for the class-AB amplifier was obtained. However, it achieved up to 29% PAE at 39 dBm P1dB. A 3 dB 2-ways 900 hybrid splitter was designed using 100 Ω impedance for optimum resistance. This is to achieve 90° phase difference between the carrier class-AB and the peaking class-AB amplifier. For a two-stage balanced PA, the carrier and peaking bias points are in the same mode, the input-output matching circuitry and the output impedances are similar as well. For the two-way splitter, various simulation tests were performed such as isolation response over the operating bandwidth, phase difference across port 1–2 and 1–3, and insertion loss response of the splitter [3]. From the 3 dB splitter design, the insertion loss achieved is reasonably low due to the high return loss, the phase difference of two signals are parallel to each other by 100 Ω, which means they are separated by 90° and have equal magnitude, and the isolation between 2 and 3, which results in −48.56 dB at 2.655 GHz centre frequency. Consequently, these results represent a response to protect the amplifier with all the instruments connected to it and allow measurement with reasonable accuracy. At the output of the two-stage amplifier is a combiner coupling the carrier and peaking amplifier signals to the output of the balanced amplifier [3, 15].

Table 1 shows the performance of the present work in comparison with a few selected PAs reported in the literature, taking account of operating frequency, output power, efficiency and gain. In [4] a power amplifier consisting of up to 54% PAE at 2.14 GHz operating frequency is presented. The design presented a two stage line-up Doherty amplifiers, consisting of a High Voltage HBT Doherty final design is cascaded with a 20 W LDMOS Doherty driver, exhibiting up to 325 W (55 dBm) power to improve the

gain to 30 dB. In the case of [10] a high power hybrid envelope elimination and restoration transmitter was design using gallium arsenide high electron mobility transistor (GaN-HEMT) at 2.655 GHz operating frequency. The design introduced a conventional hybrid switching amplifier with up to 71.2% PAE. However, the efficiency of H-EER transmitter reduced down to 37.04% at 41.18 dBm Pout. In [11] a conventional balanced amplifier with 90° branch line hybrid coupler (BLHC) was used to achieve power matching rather than maximum high gain. The impedance matching is not excellent and there is inherent out-of-phase characteristic cause from the properties of 90° BLHC. To improve the performance and correct the high signal reflection, an auxiliary amplifier was added to the conventional balanced amplifier design, only to increase the PAE to 33.4%. The design for [13] use up to 250 W output power at saturation to achieve drain efficiency of 60%. The final 40 W GaN-HEMT Doherty power amplifier design used a digital pre-distorter to enhance linearity, as a result experienced reduction in PAE to 48%. Finally, in [14] a 10 W, Si-LDMOS transistor power amplifier was presented with 50% PAE, 14.5 dB gain achieved at 41.8 dBm saturation within 1.8 to 2.0 GHz operating frequency. The drawback of [14] is that heat sink is used due to excessive heating produced by the amplifier, which extensively affect the general performance of the system.

Table 1. Performance comparisons for various power amplifiers.

Device	f_c [MHz]	PAE [%]	P_{out} [dBm]	Gain [dB]	Reference
LDMOS	2655	51	41	14.6	Balanced
LDMOS	2655	29	39	15	Class-AB
LDMOS	2140	54	48.77	30	[4]
G-HEMT	2655	37.14	41.18	12.78	[10]
G-HEMT	2125	33.4	34.9	7.7	[11]
G-HEMT	2500	48	46	13.4	[13]
LDMOS	1900	50	40	14.5	[14]

However, this work presents a simplified balanced amplifier using Si-LDMOS transistor while achieving up to 53% PAE, 14 dB gain at 41 dBm P1dB. This design is matched perfectly due to the internal input and output matching network in the transistor device. There is no evidence of leakage or signal reflection from the first stage of the design to the design of balanced amplifier. Another advantage of this design is its simplicity, requiring no auxiliary amplifier or additional cascade Doherty device to improve the efficiency. Additional circuitry accounts for extra power consumption and results in negligible impact to the overall efficiency of the amplifier [3].

3 Results and Discussion

The proposed balanced amplifier consisting of two similar class-AB amplifiers has been measured and discussed. The results show a useful extension of dynamic range with good PAE, making this approach the best choice for LTE base station applications. Figure 2 has shown the results of the balanced amplifier in comparison with conventional

class-AB amplifier. The result have shown good performance from the balanced amplifier, achieving up to 53% PAE with 14 dB gain at 41 dBm P1dB, as against the conventional class-AB amplifier with 29% PAE, 39 dBm Pout and 15 dB gain.

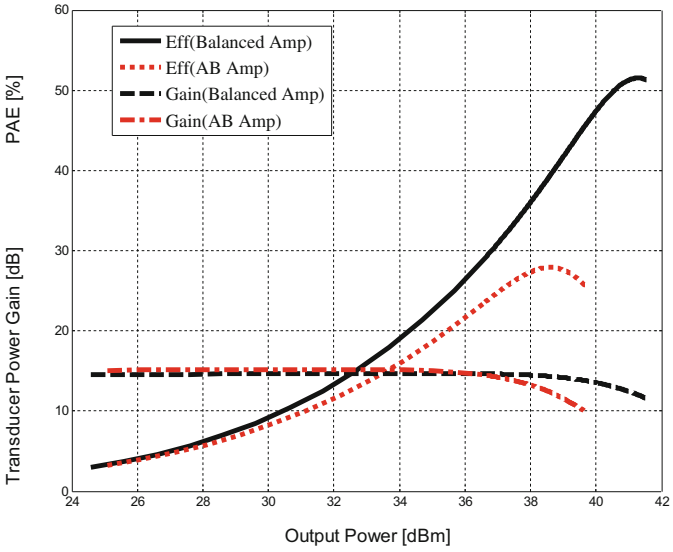

Fig. 2. PAE and gain characterization for class AB and the proposed balanced PA.

In the one-tone nonlinear simulation test, AM-AM and AM-PM characterisation parameters are also achieved as illustrated in Fig. 3. These are very important parameters in the characterisation of PA. However, the AM-AM distortion appears in a nonlinear PA, while the AM-PM distortion appears in MOSFET PAs and produce memory effects. The AM-AM and AM-PM transfer functions are used in the MATLAB curve fitting to generate coefficients. The extracted AM-AM and AM-PM data are measured in amplitude and phase in the context of normalized input voltage as a function of output voltage of the balanced amplifier. These are AM-AM extracted data, exported to the MATLAB curve fitting to generate the following coefficients: a6 = 33.066, a5 = −85.52, a4 = 82.06, a3 = −34.052, a2 = 2.85, a1 = 3.21 and a0 = −0.01. The AM-AM distortion is effected by the device reaching a saturation point. The normalized input voltage as a function of output phase of the balanced amplifier is also considered with the following AM-PM MATLAB fitted coefficients: b6 = 3.5485, b5 = −5.7836, b4 = 3.0384, b3 = −0.8434, b2 = 0.1826, b1 = −0.0225 and b0 = 0.1001. The AM-PM distortion is effected by the device reaching a saturation point. These data will be embedded in the device under test of a transmitter device, in a Simulink simulation based on IEEE 802.16 OFDM WLAN transceiver system. The polynomial functions for AM-AM and AM-PM are respectively given by the following equations:

$$y(t) = a_5u^5 + a_4u^4 + a_3u^3 + a_2u^2 + au + a_0 \tag{1}$$

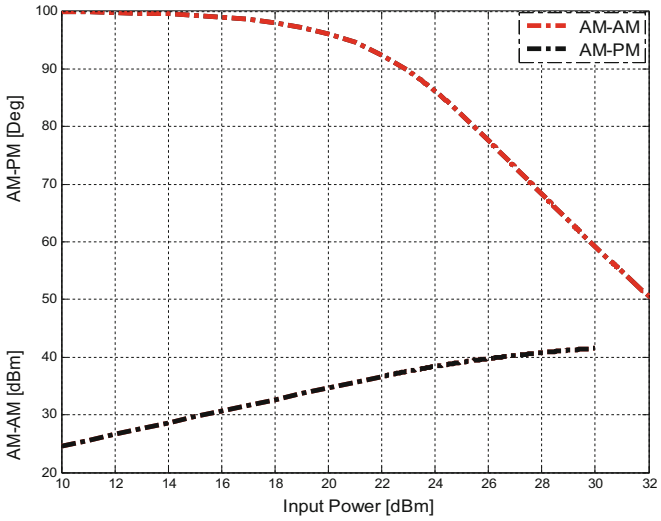

Fig. 3. AM-AM and AM-PM characterization of balanced amplifier.

$$z(t) = b_5 n^5 + b_4 n^4 + b_3 n^3 + b_2 n^2 + bn + b_0 \tag{2}$$

Simple linear formulas are presented for the functions involved in the amplitude and phase nonlinear models of the balanced amplifier, and are shown in Eqs. (1) and (2) to fit measured data very well. This model is exported to the memory-less baseband digital pre-distorter to linearize the DUT at the front-end of the OFDM transceiver system. Figure 4 illustrates results of a multiple-input-single-output (MISO) transceiver system which is set to run on simple linear model with baseband digital pre-distortion to compensate the nonlinearity of balanced power amplifier. Figure 4a and b depict AM-AM and AM-PM responses of the DUT without pre-distorter. Figure 4c and d is the same amplitude and phase results of the DUT after switching on the baseband digital pre-distorter of the transceiver system. The memory-less nonlinearity of the balanced amplifier has been compensated by the use of the digital pre-distortion mechanism. This has proven that the simple linear model used on the IEEE 802.16 OFDM WLAN transceiver system can model the AM-AM and AM-PM characteristics of the balanced amplifier.

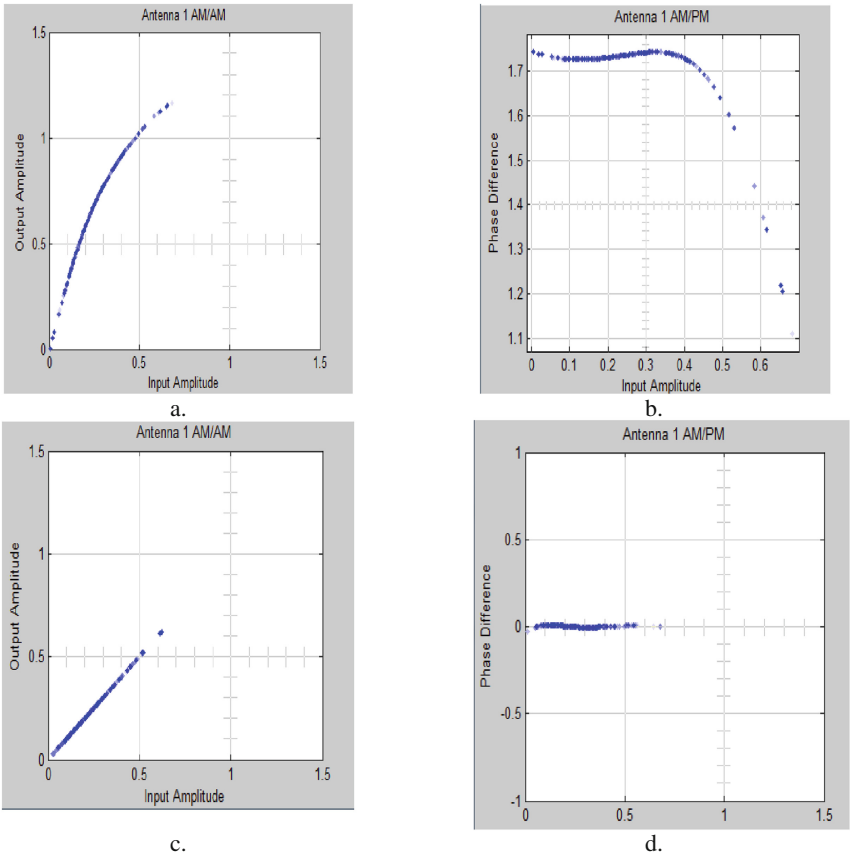

Fig. 4. a and b are the AM-AM/AM-PM responses of the DUT without pre-distortion, while c and d the pre-distortion is included.

4 Conclusion

In this paper, a balanced RF power amplifier was presented with a two class-AB amplifiers. The design used free-scale n-channel enhancement mode lateral MOSFET transistor. Linear and nonlinear simulation was achieved with ADS simulator and on the performance metric result is presented with considerable improvement. Comparison was made between the conventional class-AB amplifier and the double stage balanced RF amplifier. The balanced amplifier exhibited acceptable improvement in-terms of PAE and P1 dB by 22% and 2 dBm, with the gain decreasing by 1 dB. A relative comparison was made with power amplifiers of various types and the present work has proven a good choice of device.

This paper also conducted research on the effect of balanced amplifier AM-AM and AM-PM characteristics, when the coefficients are loaded onto the digital pre-distortion. AM-AM and AM-PM coefficients were converted to generate polynomials, using

MATLAB in the presence of a Simulink WLAN IEEE 802.16 OFDM transceiver system for pre-distortion. The pre-distortion technique was able to properly correct the nonlinear behaviour of the balanced RF power amplifier using the simple linear model to model the nonlinear characteristics of the balanced power amplifier.

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References

1. Helaoui, M., Boumaiza, S., Ghazel, A., Ghannouchi, F.M.: Low-IF 5 GHz WLAN linearized transmitter using baseband digital predistorter. In: Proceedings of the 2003 10th IEEE International Conference on in Electronics, Circuits and Systems, ICECS, vol. 1, pp. 260–263 (2003)
2. Raab, F.H., Asbeck, P., Cripps, S., Kenington, P.B., Popovic, Z.B., Pothecary, N., et al.: Power amplifiers and transmitters for RF and microwave. IEEE Trans. Microw. Theory Tech. **50**, 814–826 (2002)
3. Mohammed, B.A., Abduljabbar, N.A., Abd-Alhameed, A.A., Hussaini, A.S., Nche, C., Fonkam, M., et al.: Towards a green energy RF power amplifier for LTE applications. In: Internet Technologies and Applications (ITA), Wrexham, pp. 388–392 (2015)
4. Page, P., Steinbeiser, C., Landon, T., Burgin, G., Hajji, R., Branson, R., et al.: 325 W HVHBT Doherty final and LDMOS Doherty driver with 30 dB gain and 54% PAE linearized to −55 dBc for 2c11 6.5 dB PAR. In: IEEE Circuit Symposium in Compound Semiconductor Integrated (CSICS), pp. 1–4 (2011)
5. Hussaini, A.S., Sadeghpour, T., Abd-Alhameed, R., Child, M.B., Ali, N.T., Rodriguez, J.: Optimum design of Doherty RFPA for mobile WiMAX base stations. In: Rodriguez, J., Tafazolli, R., Verikoukis, C. (eds.) MobiMedia 2010. LNICSSITE, vol. 77, pp. 700–705. Springer, Heidelberg (2012). doi:10.1007/978-3-642-35155-6_59
6. Deguchi, H., Ui, N., Ebihara, K., Inoue, K., Yoshimura, N., Takahashi, H.: A 33 W GaN HEMT Doherty amplifier with 55% drain efficiency for 2.6 GHz base stations. In: IEEE MTT-S International in Microwave Symposium Digest, pp. 1273–1276 (2009)
7. Wang, Z.: Demystifying envelope tracking: use for high-efficiency power amplifiers for 4G and beyond. IEEE Microwave Mag. **16**, 106–129 (2015)
8. Deguchi, H., Watanabe, N., Kawano, A., Yoshimura, N., Ui, N., Ebihara, K.: A 2.6 GHz band 537 W peak power GaN HEMT asymmetric Doherty amplifier with 48% drain efficiency at 7 dB. In: IEEE MTT-S International Microwave Symposium Digest (MTT), pp. 1–3 (2012)
9. Ismail, A.A., Younis, A.T., Abduljabbar, N.A., Mohammed, B.A., Abd-Alhameed, R.A.: A 2.45-GHz class-F power amplifier for CDMA systems. In: Internet Technologies and Applications (ITA), pp. 428–433 (2015)
10. Ildu, K., Junghwan, M., Jangheon, K., Jungjoon, K., Cheol Soo, Kae-Oh, S.S., et al.: Envelope injection consideration of high power hybrid EER transmitter for IEEE 802.16e mobile WiMAX application. In: IEEE MTT-S International Microwave Symposium Digest, pp. 411–414 (2008)
11. Jongsik, L., Chunseon, P., Jakyung, K., Hyeonwon, C., Yongchae, J., Sang-Min, H., et al.: A balanced power amplifier utilizing the reflected input power. In: IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), pp. 88–91 (2009)

12. Markos, A., Bathich, K., Tanany, A., Gruner, D., Boeck, G.: Design of a 120 W balanced GaN Doherty power amplifier. In: Microwave Conference (GeMIC), German, pp. 1–4 (2011)
13. Sano, H., Ui, N., Sano, S.: A 40 W GaN HEMT Doherty power amplifier with 48% efficiency for WiMAX applications. In: IEEE Symposium in Compound Semiconductor Integrated Circuit (CSIC), pp. 1–4 (2007)
14. Dai, D., Sun, L., Wen, J., Su, G., Guo, L.: A 10 W broadband power amplifier for base station. In: 2012 International Conference on Microwave and Millimeter Wave Technology (ICMMT), pp. 1–4 (2012)
15. Kim, S., Moon, J., Lee, J., Park, Y., Minn, D., Kim, B.: Mitigating phase variation of peaking amplifier using offset line. IEEE Microwave Wirel. Compon. Lett. **2**, 1–3 (2016)