Wireless Power Transfer for Energy-Efficient Electric Vehicles

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Abstract. This paper presents the wireless power transfer (WPT) technology based on inductive coupling and the design challenges of a hybrid energy harvester (EH) circuit as a promising solution to promote the energy efficiency of the electric vehicles (EVs). The design methodologies of ultra-low power electronic module based on low leakage conditioning and processing device are details based on nanoscale transistor technology so that the WPT and hybrid EH can be implemented for self-powered devices in EVs.

Keywords: Adaptive back-gate biasing · Electric vehicles · Energy harvester · Ultralow power design · Wireless power transfer

1 Introduction

The share of electronic component by the high integration of more sensors and actuators in the EVs is fast growing and plays a decisive role not only in satisfying primary customer wishes for better driving safety (vehicle stability in windy or rainy environment) and comfort such as entertainment applications (i.e. music, video), but at the same time to achieve better electric energy economy [1]. Moreover, the contribution of numerous digital, analog, and mixed signal processing transceivers as well as the high-integration of electronic control units (ECUs), high definition screens makes the embedded devices much more energy hungry in EVs [2–4]. Many of these functions has to be designed and implemented considering the wireless data exchange between electronic components and the optimizing the energy consumption to prolong the EV's battery autonomy.

The wireless power transfer (WPT) technology and energy harvesting present the effective solution to energy-efficient EVs to stay competitive in the market share [2–5]. The WPT based on inductive coupling mechanisms and the design principles for green EVs based on self-powered micro-electro-mechanical systems (MEMS) and their implementation in a most cost-effective way play an important role in order to improve energy efficiency and reduce greenhouse gas emissions in the sustainable transport sector [4–6]. The remains of this manuscript is organized as follows. Section 2 describes the inductive coupling mechanism and its performance in promoting not only

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the WPT for powering the EV's sensor or actuator but also communication between vehicle's wireless sensor networks. Section 3 presents low static power design techniques through back-gate biasing design methodologies enabled by the new nanoscale transistor technology without sacrificing chip's speed while detailing the back-gate biasing mechanisms and effects and presenting the fundamental techniques to reduce leakage power. Finally, conclusions are drawn in Sect. 4.

2 Wireless Power and Data Transmission

2.1 Inductive and Radiative Coupling

Self-powered electronic devices (i.e. processors, sensors, and actuator) are free of cables and have freedom mobility during charging and usage. The device's charging use the WPT principle which is based on a magnetic resonance coupling. Inductively coupled systems are based upon a transformer-type coupling between the primary and the secondary coils (antenna). For instance, radio frequency identification (RFID) is a wireless communication technology based on the WPT principle of mutual induction used for in-vehicle communication but can be used also for near field communication between close vehicles or for localization purpose [5] as shown in Fig. 1.

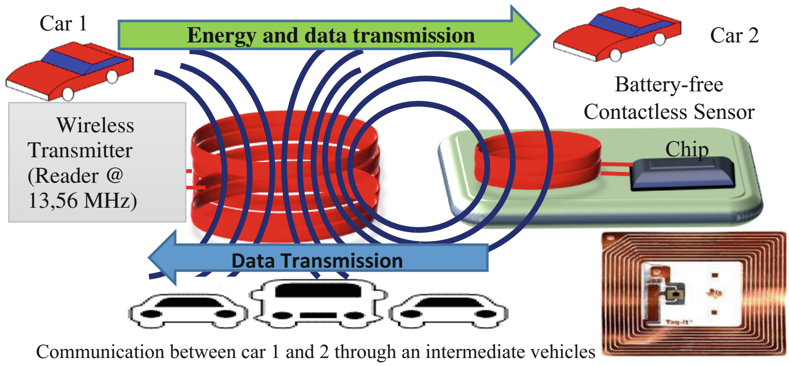

Fig. 1. Inductive coupling for wireless power and data communication between vehicles.

The RFID device of the first car is self-powered by the received electromagnetic wave and is capable of communicating data with reader of the second car that modulates the RF signal that is coming from the reader. The power consumption on the reader is minimized because there is no RF section embedded in the chip and the information is communicated through load modulations [4, 5]. The RFID and inductively coupled devices may be modelled, as a first approximation by the circuit shown in Fig. 2 where L_1 and L_2 represent the inductance of the transmitter and receiver antenna, respectively. R_1 and R_2 are the antenna's coil resistances. The current consumption of the data memory is modeled by the load resistor R_L. A time varying

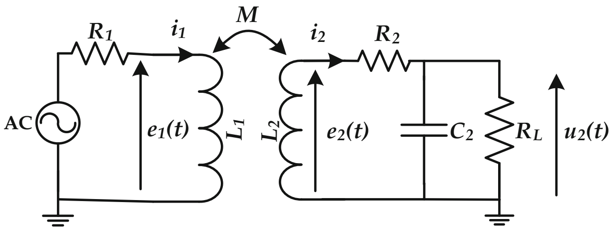

Fig. 2. Equivalent circuit diagram for magnetically coupled conductor loops

modulated magnetic field in the coil L_1 induces voltage $u_2(t)$ in the coil loop L_2 due to mutual inductance M. The flow of current creates an additional voltage drop across the coil resistance R_2.

Under sinusoidal RF approximation, the induced voltage in the receiver coil:

$$U_2(j\omega) = \frac{j\omega M I_1(j\omega)}{1 + \frac{(j\omega L_2 + R_2)}{R_L}} \tag{1}$$

The voltage $u_2(t)$ induced in the receiver coil is used to provide the power supply to the data memory (microchip). In order to significantly improve the WPT efficiency, an additional capacitor C_2 is connected in parallel with the receiver's coil L_2 to form a resonant circuit at frequency of the RFID system (i.e. $f_{RES} = 13.56\,\text{MHz}$). The required capacitance for the capacitor C_2 is found by taking into account the parasitic capacitance C_p (e.g. $C_2 = 1/\omega^2 L_2 - C_p$). Thus obtaining the relationship between voltage u_2 and the magnetic coupling of transmitter coil and transponder coil [5].

$$U_2(j\omega) = \frac{j\omega k\sqrt{L_1 L_2} I_1(j\omega)}{1 + (j\omega L_2 + R_2)\left(\frac{1}{R_L} + j\omega C_2\right)} \tag{2}$$

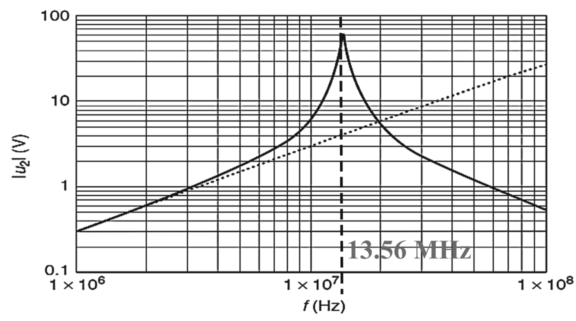

Fig. 3. Magnitude of the received voltage versus frequency. A transponder coil with a parallel capacitor (continuous line) (dashed-line: coil without a resonant capacitance).

2.2 Wireless Power Transfer

A wireless charging system enable EVs to be continuously charged with unlimited driving range. As shown in Fig. 4(a), WPT is used to wirelessly transmit large electric currents between metal coils of the high way and the EVs [2, 6]. The variable capacitor bank in the power transmitter and receiver in used to ensure the maximum WPT at the resonance frequency. Design cost to develop all electric highway will be increased with many transmitters in a given length of the track. Several transmitter coils can be connected to a single power converter in parallel. Figure 4(b) shows equivalent circuit considering various nearby transmitters which are separately powered [1].

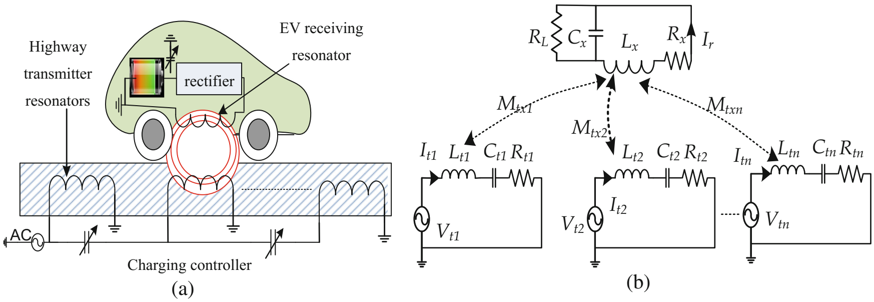

Fig. 4. (a) Magnetic fields (red) continuously and wirelessly charge EVs. (b) Equivalent circuit of EV charging considering separated powered n transmitters. (Color figure online)

Kirchhoff circuit laws allow establishing this system of linear equation that can be determined with respect to the unknown currents vector and to determine the power transfer efficiency (PTE) [1].

$$\begin{bmatrix} Z_{t_1} & 0 & \dots & 0 & X_{t_1r} \\ 0 & Z_{t_2} & \dots & 0 & X_{t_2r} \\ 0 & 0 & \ddots & Z_{t_n} & X_{t_nr} \\ X_{rt_1} & X_{rt_2} & \dots & X_{rt_3} & (Z_r + R_L) \end{bmatrix} \begin{bmatrix} I_{t_1} \\ I_{t_2} \\ I_{t_n} \\ I_r \end{bmatrix} = \begin{bmatrix} V_{t_1} \\ V_{t_2} \\ V_{t_n} \\ 0 \end{bmatrix} \tag{3}$$

$$PTE = \frac{P_{out}}{P_{in}} = \frac{R_L |I_r|^2}{R_{t_1}|I_{t_1}|^2 + R_{t_2}|I_{t_2}|^2 + R_{t_n}|I_{t_n}|^2 + (R_r + R_L)|I_r|^2} \tag{4}$$

The self-impedances, $Z_k = R_k + j(\omega L_k - 1/\omega C_k)$, of transmitter $k \in (t_1, t_2, \dots, t_n)$ or the receiver (r) coils are composed of the inductance, L_k, the resistance R_k of the coil, and the capacitance, C_k. $X_{jk} = X_{kj} = j\omega M_{jk}$ where $M_{jk} = M_{kj}$ is the mutual inductance between k^{th} coil and j^{th} coil, k and $j \in \{t_1, t_2, \dots, t_n, r\}$.

2.3 Hybrid Energy Harvester

EH is an appealing and promising solution to improve the energy-efficiency of EVs. The hybrid EH focus on the electronic design of an ultra-low power (ULP) embedded devices to be powered from renewable and multiple energy sources (e.g. solar, thermal, vibration, RF signals). Firstly, ambient RF signals become widely and frequently present over an increasing range of frequencies and power levels, including mobile telephones, mobile base stations, and television/radio broadcast stations, especially in highly populated urban areas that harvest hundreds of microwatts that will potentially enable users to provide self-powered devices based in scavenged RF signals [7]. For instance, Powercast demonstrated ambient RF energy harvesting at 1.5 miles (~2.4 km) from a 5 kW AM radio station [8, 9]. While the amount of the harvested RF energy source is appropriate to bias small sensor, it is insufficient to fulfil the ECU energy requirements. Therefore, additional renewable energy in conjunction with harvested RF energy is needed to be integrated in the hybrid EH. This will lead to significantly save the electric energy and prolong the autonomy of the battery [9]. Harvesting energy from vibration use piezoelectric materials to convert mechanical strain into useable electrical energy. The piezoelectric transducer used in conjunction with a power conditioning circuit, which converts the AC output to a regulated DC output. Heat can also be easily harvested in EV. The thermoelectric generators transducer, due to the high temperature gradient and allied materials, capture waste heat in vehicles and convert it to electricity needed to power wireless sensors and transmit data or to charge batteries that run ECU.

The architecture of the adaptive multisource EH is shown in Fig. 5. This ECU of the power management module enable the multisource energy monitoring and provide control capability that will be applied to the shared maximum power point tracking (MPPT) circuit, which dynamically adjusts the operational parameters of the energy conversion devices in response to the variations of energy sources so that the output power is maximized. The rectifier circuit in the RF and vibration EH is used to convert the alternate output current at millimetre wave frequency and low frequency, respectively, into DC. In addition, a battery is used for storing a possible energy surplus.

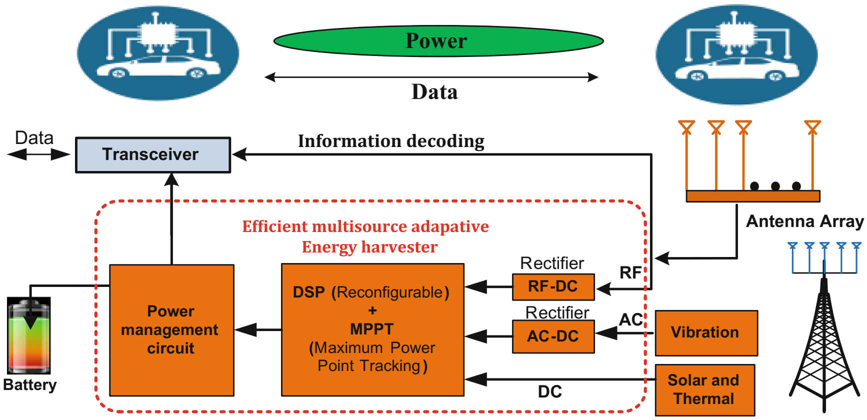

Fig. 5. Efficient Vehicle hybrid harvesting circuit

Although traditional devices are battery powered that are replaced every 3 to 5 years, electronic systems in energy-efficient EVs can be self-powered such as light adjustment systems and tire pressure monitoring systems (TPMS). For instance, MEMS-based piezoelectric EH devices is used to generate enough power (40 μW) based on the vibration's energy captured from the wheels when the car is in motion. This energy is converted to voltage that powers both the pressure sensor and the wireless communications circuitry to bias the TPMS.

Designing EVs electronic devices using ULP operation is important to prolong the battery lifetime. Legacy battery technology is finite and has not evolved at the same rate as the ultra-low power and high-speed very large scale integration for chips design, which is driven by Moore's law. Therefore, as EVs become more sophisticated, an energy trap is emerging where power demand starts to vastly exceed actual power supply. This provides an impetus for EVs stakeholders to envisage new technologies to drive future energy-efficient EVs for longer and sustainable periods of time [8].

3 Ultra-Low Power and High-Speed Chip Design

Wireless charging by means of hybrid EH and WPT requires an improved performance of low-leakage electronics design and energy storage devices in order to continuously decrease in the power consumption of electronic components. Since, the leakage current strongly depends on the threshold voltage, V_{TH}, different V_{TH} transistors can be used for speed and power tradeoff [10].

3.1 Downscaling Challenges in Bulk Technology

Transistor dimensions have been downscaled to reduce the cost, minimizing the capacitance. Moreover, the V_{dd} and V_{TH} tend to be scaled by same factor to limit current degradation. Also, the short channel effects (SCE) have a direct impact on the V_{TH} which has resulted in an exponential increase the contribution of the off-state leakage current in the total power dissipation of a bulk CMOS system as shown in Fig. 6a [11]. These consequences have moved the bulk technology to a power constrained condition.

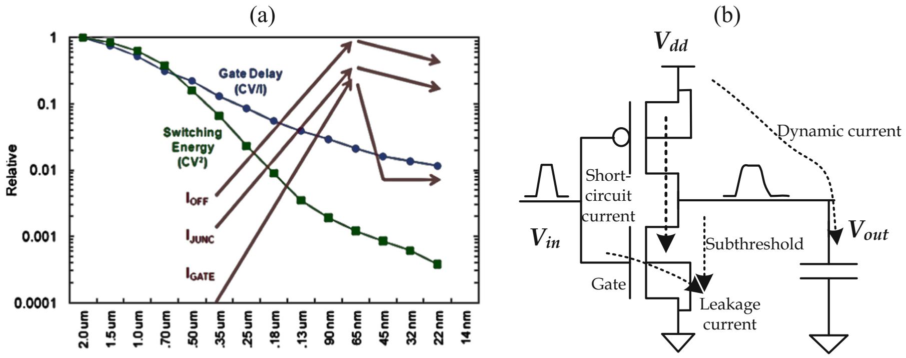

Fig. 6. (a) Ratio of active, leakage powers, and the gate delay over the CMOS technology [11]. (b) The dynamic and static (leakage) currents associated with a CMOS device.

The CMOS power consumption can be divided into three components. The dynamic and short-circuit power are consumed while the input switches. The static leakage power is consumed due to the transistor's sub-threshold, gate and diode junction's currents while the input is kept constant as shown in Fig. 6b.

$$P_{total} = \alpha \cdot C \cdot V^2 \cdot f_{clk} + V_{dd} \cdot I_{sc} + V_{dd} \cdot I_{Leakage} \tag{5}$$

The first and second terms in (5) refer to the dynamic power which represents the switching and short circuit power, P_{sw}, P_{sc}, respectively. P_{sw} is determined by the activity factor, α which is the the fraction of the circuit that is switching under the supply voltage V_{dd}, the clock speed, f_{clk}, and the equivalent switching capacitance, C. P_{sc} is consumed when both the pull up and pull down network of the logic gate circuit partially conduct as illustrated in Fig. 6b. The V_{TH} is a fundamental parameter in circuit design and testing. The transistor sub-threshold output current, I_{DS}, which is important to keep it very small in order to minimize the standby (i.e. sleep) mode. Moreover, the drain current increases exponentially on the V_{GS} [10, 12].

$$I_{DS,sub} \propto \exp\left(\frac{q.V_{GS}}{n.K.T}\right) \tag{6}$$

where K is the Boltzmann constant, T is the absolute temperature, q is the electron charge, and the sub-threshold slop n depends on the capacitance of the CMOS technology. It is worth to note that a higher I_{ON} maximizes the circuit speed because it reduces the charging time of the pad capacitances. This higher I_{ON} can be achieved by a lower V_{TH}. However, lowering V_{TH} increases exponentially the leakage current. This is the tradeoff between speed and power that the designer should balance [11, 13].

3.2 New Transistor Technology

The transistor V_{TH} can be controlled by the potential of the body terminal contact [12].

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \tag{7}$$

where γ is the body effect coefficient, ϕ_F is the Fermi potential, and V_{TH0} is the zero threshold voltage while source-bulk bias is equal to 0 ($V_{SB} = 0$). γ describes the changes (e.g. shifting) in the V_{TH} by varying the V_{SB} voltage. It can be consider as a second gate and is sometimes referred to as the "back gate" that helps to determine how fast the transistor turns on and off. Strong γ enables a variety of effective body biasing techniques that were effectively used in older process generations. However, body effect has diminished with Bulk nanoscale transistor [12]. From transistor architecture and materials perspectives, breakthroughs were needed to reduce the SCE and the leakage currents in sub-28 nm bulk CMOS technology process and to decrease the capacitance factor. The Fin-type field-effect transistors (FinFET) and fully depleted silicon-on-insulator (FDSOI) technology provides the promising new transistor technology to do back-gate biasing effects. In addition, the SCE in an ultra-thin body

FDSOI MOSFET can be suppressed by thinning down the silicon body and buried oxide (BOX) thickness that lead to a double-gate device structure on SOI substrate. This Ultra-thin body and BOX (UTBB) FDSOI transistor architecture has a stronger γ than conventional transistors and therefore enables effective V_{TH} management through body biasing. It is worth to note also that double-gate transistor structures such as the vertical (3D) FinFET are more challenging to manufacture than the planar (2D) FD-SOI MOSFET structure as shown in Fig. 3 [12, 13]. The range of back-gate biasing in UTBB FDSOI is quite wider (i.e. $-3\,\mathrm{V} < V_{SB} < 3\,\mathrm{V}$) by a factor of 10 compared to the bulk technology (i.e. $-300\,\mathrm{mV} < V_{SB} < 300\,\mathrm{mV}$) due to the transistor structure as shown in Fig. 7. Back-biasing consists of applying a voltage just under the BOX target of the UTTB FDSOI transistors that changes the electrostatic control of the transistors and shifts their V_{TH}, as shown in Fig. 8, to speed up the switch at the expense of increased leakage current or reduce it at the expense of speed degradation [12].

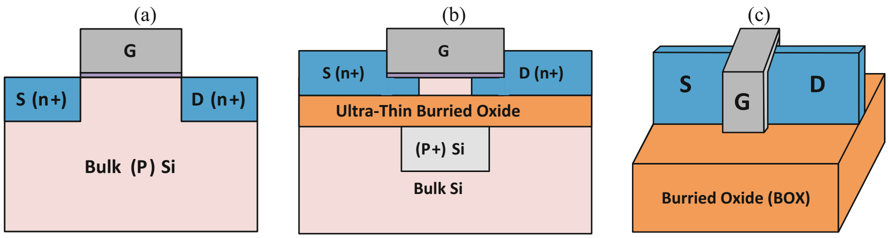

Fig. 7. Structure of different transistor technology: (a) Conventional Planar Bulk Transistor, (b) Planar Single-or double Gate FDSOI, (c) Vertical Multiple-Gate FinFET SOI [12].

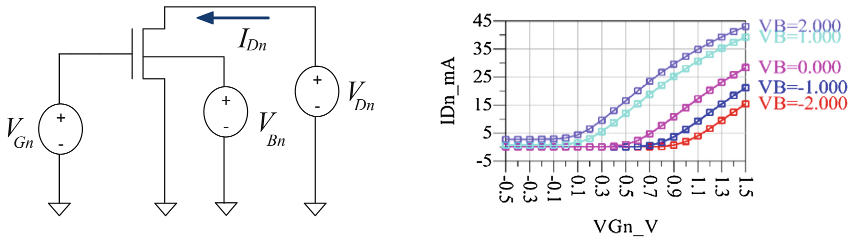

Fig. 8. Shifting effects on the V_{TH} introduced by the back-gate biasing n-channel UTTB FDSOI.

3.3 Multiple Threshold Biasing

The multiple threshold biasing technique employs the low-V_{TH} transistors to design the logic gates for which the switching speed is essential, and the high-V_{TH} transistors (also called sleep transistors) to effectively isolate the logic gates in the standby state and reduce the leakage dissipation. The generic circuit structure of the multiple threshold design circuit is offered in Fig. 9b. The sleep transistors are controlled by the sleep

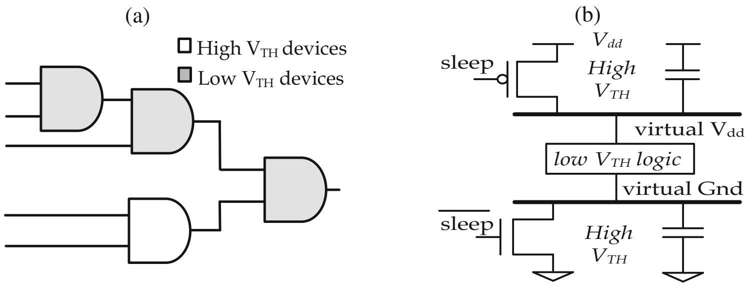

Fig. 9. (a) Dual-V_{TH} partitioning and (b) Multiple threshold design scheme [13].

signal. During the active mode, the sleep signal is enabled, causing both high-V_{TH} transistors to turn on and provide a virtual power and ground to the low-V_{TH} logic. When the circuit is inactive, sleep signal is disabled which forces both high-V_{TH} transistors to cut-off and disconnect the power lines from the low-V_{TH} logic. This results in a very low leakage current from power to ground when the circuit is in standby mode.

3.4 Adaptive and Dynamic Back-Gate Biasing

Adaptive body bias is a valuable tool for overcoming systematic manufacturing variation, which is usually manifested in the handled devices as leakage or timing variation between chips. This undesirable current can be controlled adaptively through a body-bias circuit generator that is connected to the back-gate of the low-V_{TH} SOI nMOS and pMOS transistors as shown in Fig. 10. This dynamic control enable to dynamic shift of V_{TH} during its operation, rather than setting the body bias just once either during design or at production test, in order to either lower the V_{TH} when needing more speed, or raise it when running at lower speeds to optimize the leakage power. Consequently, dynamic body bias can be used to compensate the process variation related to the temperature, aging effects, and to efficiently manage power modes [14].

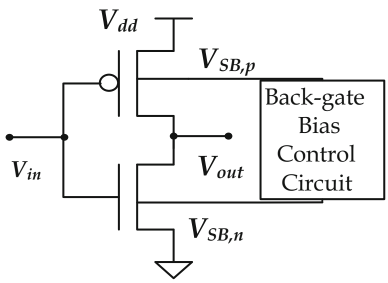

Fig. 10. Adaptive biasing scheme of low-V_{TH} and low-V_{DD} UTTB FSOI Inverter.

During the active mode the transistors circuit of Fig. 6 work as conventional CMOS transistors without back-gate biasing. As the circuit enters to the standby state, the back-gate bias control circuit generates a lower $V_{SB,n}$ for the SOI nMOS transistor and a higher $V_{SB,p}$ for the SOI pMOS transistor. As a result, the magnitudes of the respective threshold voltages $V_{TH,p}$ and $V_{TH,p}$ both increase in the standby mode due to the back-gate effect. Therefore, the leakage power dissipation in the standby state can be significantly reduced with this circuit design technique.

4 Conclusions

Highly resonant inductive coupling mechanism enable the wireless power and data connectivity between EVs that are becoming more connected and autonomous. Constructing an automated highway system and infrastructure where wirelessly EVs are charged and using a hybrid EH integrating multiple renewable energy sources will make the EVs more energy-efficient and will improve the flow of traffic by introducing more self-powered sensors and actuator while lowering greenhouse gas emissions and prolonging the battery lifetime of EVs.

Competitive energy-efficient EVs requires an improved performance of low-leakage electronics design in order to continuously decrease in the power consumption of electronic components. Therefore, the recent progress in nanoscale technology by investigating the FinFET and the UTBB FDSOI revive the ability of higher back-gate bias effect by enabling wider range of back voltage to adjust the V_{TH} according to the circuit specifications. Also, it brings a significant improvement in terms of speed, dynamic power saving and flexibility to static leakage power management design techniques for energy efficiency optimization during early silicon stage design or at the post-silicon stage by tuning the chip's bias for process compensation.

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