Flexible In-Band Full-Duplex Transceivers Based on a Modified MIMO RF Architecture

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Abstract. In-band full-duplex transceivers are considered for future generations of cellular network systems. This paper proposes to evaluate the performance of in-band full-duplex transceivers using a modified architecture based on hardware available for multiple-input multiple-output transceivers. A hybrid self-interference cancellation technique using an auxiliary transmitter is therefore introduced. Performance is evaluated using simulation models and is confirmed by hardware experimentation. The main limiting factors of the proposed architecture are analyzed and improvements to the architecture are then suggested.

Keywords: In-Band Full-Duplex · Transceiver · MIMO architecture · RF impairments

1 Introduction

The massive adoption of smartphones together with the need to always be connected has accelerated the demand for broadband mobile connectivity. Therefore, the capacity of cellular networks should continue to increase to meet end-user requirements. A possible solution considered by cellular operators is to further improve spectral efficiency. Multiple Input Multiple Output (MIMO) techniques [1, 2] and relay techniques [3, 4] which have been studied for the last twenty years allow cellular operators to improve bit rate and capacity. Another alternative consists in increasing the useful bandwidth or in deploying new locations for base stations. All options increase the cost and/or the power consumption of the base station or the mobile equipment. Recently In-Band Full-Duplex (IBFD) solution has been studied and demonstrated in the Wireless Local Area Network (WLAN) context [5–8]. It seems to be a promising approach to resolve the asymmetric data flows introduced by Frequency Division Duplex (FDD) communication or to reduce latency in Time Division Duplex (TDD) communication. It may optimize time-frequency resources and can under certain conditions increase the overall capacity [9].

Basically, the main problem of IBFD transceivers is self-interference. In a full-duplex point-to-point communication, both transmitters and receivers simultaneously transmit and receive in the same frequency band. Therefore each transmitter generates a powerful signal which simultaneously creates a well-known self-interference at the receiver. To receive the useful low power signal, the transceiver must cancel this self-interference.

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Several methods can be used to cancel the self-interference but all request a cancellation in the analog domain. This can be done at the antenna level and at RF level. The important level of cancellation that is required cannot be only reached in the digital domain mainly because of the analog-to-digital converter which does not support such a dynamic range.

In 2013, Stanford proposed a new IBFD architecture based on a single antenna with circulator, a digitally controlled broadband analog filter and a digital canceller [8]. Stanford demonstrated an IBFD single input single output (SISO) transmission at 2.4 GHz. The full-duplex transceiver was able to reject self-interference level of around 110 dB over 80 MHz of bandwidth. A first RF cancellation step of 62 dB is provided by a circulator and a broadband analog filter. Then, a digital canceller adds 48 dB of cancellation. The overall transmitted signal of 20 dBm was reduced to the thermal noise level of −90 dBm. The main contributions of Stanford are the broadband analog filter and the digital canceller that takes into account the non-linear effect.

The solution proposed by Stanford [8] is very performant but very complex especially the digitally controlled analog filter. This analog filter consists in 16 delay lines with 16 attenuators controlled by 7 bits command for a range of 31.75 dB and successive steps of 0.25 dB. The Peregrine Semiconductor attenuator components used in this analog broadband filter are not perfect. The RF attenuation is not exactly the expected attenuation, the relative phase changes when the attenuation or frequency increases [10]. This supposes a calibration process. Moreover the delay lines need to be adapted to the frequency band and the antenna structure.

The next section introduces the proposed architecture. Part III presents the self-interference cancellation technique and its performance. In part IV, the canceller is evaluated through a simple implementation on real signal.

2 Flexible Architecture

In this paper, an alternative architecture is studied in order to reduce the complexity of the analog broadband filter proposed by the Stanford solution. The envisaged solution is based on current RF MIMO transceiver architectures. As previously mentioned, current generations of cellular systems support MIMO communication, meaning that most of the transceiver supports multiple transmitters. In this paper we will try to evaluate a full-duplex architecture using these multiple transmitters. The second transmitter called auxiliary transmitter will replace the broadband analog filter. It is called Hybrid Self-Interference Cancellation (HSIC). In our context, the target requirements are less ambitious than the Stanford requirements but our solution is simpler to integrate and updates from current device architectures. The MIMO FDD transceiver becomes a single ended IBFD transceiver. This proposal allows the Radio Resource Management (RRM) to select between classical FDD MIMO or IBFD single-end transmissions. The transceiver becomes flexible and can switch from a configuration to another according to the scenario. If the channel conditions as well as the interference environment are favourable for MIMO transmission, MIMO operation is selected. Otherwise IBFD can be considered. Impact of coexistence between MIMO and IBFD will not be studied in this paper. Few components are added compared to a classical MIMO transmit architecture. The rest of the transceiver does not change. Only

the baseband takes the self-interference cancellation into account. This evolution corresponds to a smaller technology gap than previously thought architectures and should make the migration to IBFD more acceptable. The overall flexible architecture is presented in Fig. 1.

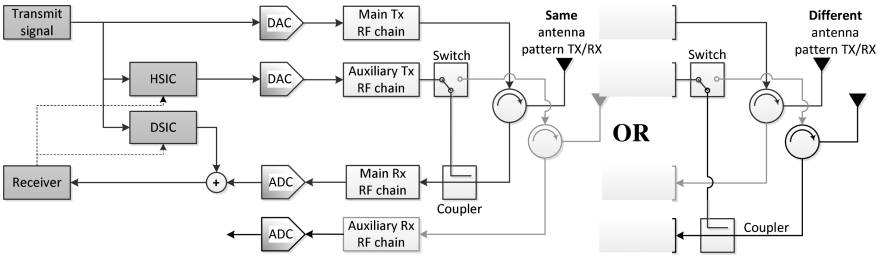


Fig. 1. In-band Full-duplex transceiver using MIMO architecture

3 Theoretical Study

3.1 Overview

This section presents the simulation model. It is used for performance evaluation of the interference cancellation technique. This simulation chain consists of several blocks. Each block models component of the transceiver taking into account most of the imperfections. We chose models for converters (i.e. DAC and ADC), phase noise of local oscillators, amplifiers non-linearities, circulator and antenna matching and isolation. Most of the models can be found in reference [11]. In this theoretical study, we focus our effort on the impact of the transmitter noise and the transmitter non-linearity on the performances. Baseband equivalent models have been considered.

3.2 Models

The model used for quantization, phase noise, Low Noise Amplifier (LNA) and converters are presented in [11]. Time varying effects have not been considered. For Power Amplifier (PA), we use the same model as [11] regarding the amplitude non-linearity and we chose the Saleh model [12] for the phase distortion:

$$\varphi_{out} = \varphi_{in} + \frac{\alpha_{\varphi}|x_{in}|}{1 + \beta_{\varphi}|x_{in}|^2} \tag{1}$$

Where φ_{out} is the phase of the output signal of the PA and φ_{in} its phase at the input. α_{φ} and β_{φ} are the parameters of the model and $|x_{in}|$ is the input signal's magnitude. To model the complex transfer function of the circulator, the S-parameters of a 2.4 GHz circulator connected to an antenna have been measured. The measured response is then

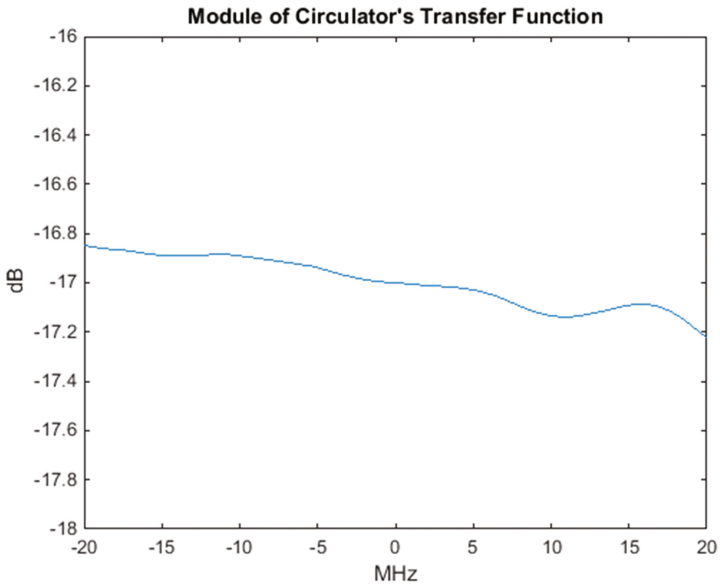


Fig. 2. Equivalent baseband circulator and antenna frequency response

translated to baseband for simulation and given in Fig. 2 for reference. Note that this response includes the reflection coefficient of the antenna.

The filters used in the simulation are 3rd-order Butterworth-type Infinite Impulse Response (IIR) filters. The developed simulation can be applied in baseband or with a transposition to an Intermediate Frequency (IF).

3.3 Hybrid Analog and Digital Self-interference Cancellation HSIC

The analog canceller aims at reducing the linear contribution of the self-interference and avoids the ADC saturation. It is in fact a hybrid analog-digital solution, as defined in [13]. It is based on an auxiliary synchronous transmitter. From the digital baseband domain, the auxiliary RF transmitter generates an analog signal which is subtracted from the main reception path. Please note that the RF components of the first and second transmitters are identical nevertheless the circulator on the main transmitter and the coupler introduces important mismatches. In practice, these mismatches must be estimated and compensated to optimize the analog cancellation performances. The filters to be estimated correspond to the h_{t1} and h_{t2} on Fig. 3.

If linearity is assumed, the signal at the output of the analog canceller is given by:

$$y_a(t) = (x_1 * h_{t1})(t) - (x_2 * h_{t2})(t) + r(t) \tag{2}$$

Where x_1 and x_2 are the outputs of the digital transmitters, r is the received signal coming from the antenna and $*$ being the convolution product.

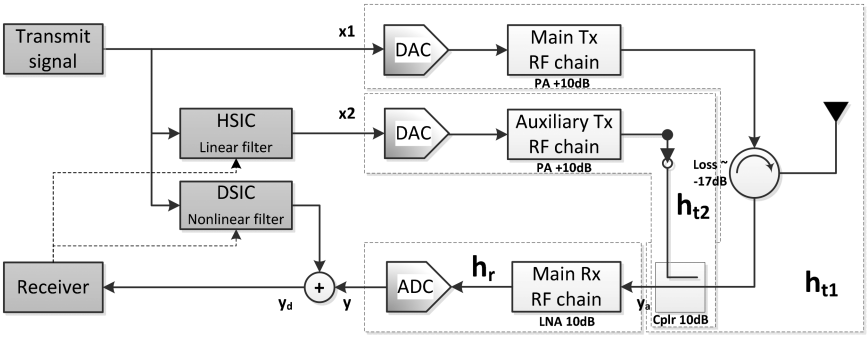


Fig. 3. Schematized system with transmission filters

The linear contribution of the self-interference at the output of the analog canceller is given by:

$$self\_interf(t) = (x_1 * h_{t1})(t) - (x_2 * h_{t2})(t) \tag{3}$$

Therefore to minimize the self-interference, the following equality should be reached:

$$\frac{X_2(f)}{X_1(f)_2} = \frac{H_{t1}(f)}{H_{t2}(f)} \tag{4}$$

Where $X_1(f)$, $X_2(f)$, $H_{t1}(f)$ and $H_{t2}(f)$ are respectively the Fourier transforms of x_1, x_2, h_{t1} and h_{t2}. Only the discrepancy between h_{t1} and h_{t2} is important. This difference is estimated in a two-step calibration measurement. Firstly, the filter between x_1 and y (denoted h_1) is estimated when nothing is transmitted on the auxiliary path. Secondly, the filter between x_2 and y (denoted h_2) is estimated when nothing is transmitted on the main path. The signal x_2 is derived from h_1, h_2 and x_2 as follows:

$$x_2(k) = x_1(k) * TF^{-1}\left(\frac{H_{t1}(f)}{H_{t2}(f)}\right) = x_1(t) * TF^{-1}\frac{H_1(f)}{H_2(f)} \tag{5}$$

As

$$H_i = H_{ti}H_r \text{ for } i = 1, 2 \tag{6}$$

Where TF^{-1} is the inverse Fourier transform. Filters h_1 and h_2 are estimated thanks to a reference sequence in the time domain as mentioned in the reference [8].

3.4 Digital Non-linear Self-interference Cancellation DSIC

The digital cancellation objective is to remove the remaining self-interference. As previously mentioned, the analog cancellation does not consider non-linear terms, so

the digital cancellation is needed to take care of the nonlinear contribution [8]. Only non-linear terms of odd orders can interfere in the useful frequency band [11]. Considering these non-linear terms, we have:

$$y(k) = \sum_{m\,odd, k=-n,\ldots,n} x(k)(|x(k)|)^{m-1} * h_m(k) \tag{7}$$

The considered filter estimation technique is similar to the one of the hybrid analog part, is realized for each order m.

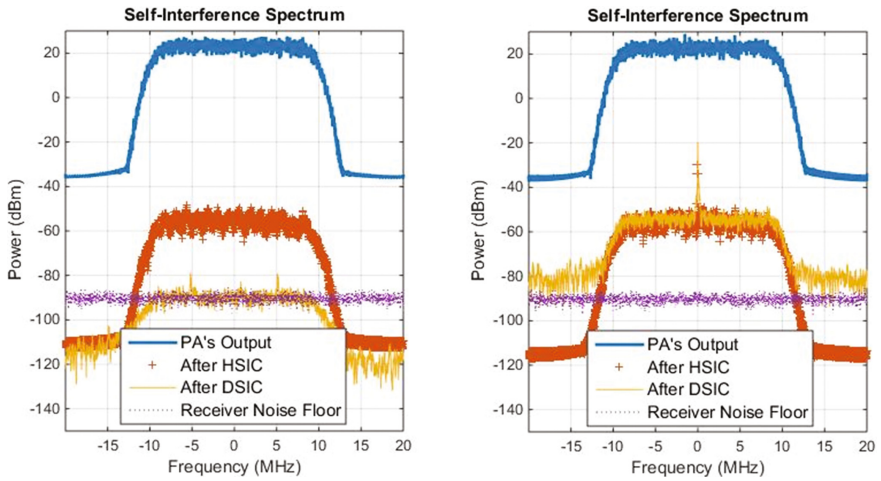
The studies consider lower non linearity effect on the auxiliary RF transmitter. This assumption is supposed to be right if the circulator isolation is important compared to the coupling factor. In this case, the hybrid canceller asks for an output power of the auxiliary chain lower than the main transmitter. The nonlinear contribution comes from the main RF transmitter, the circulator and the RF receiver.

3.5 Performances

The performances of the system are characterized by the self-interference after the HSIC and finally after the DSIC. In the simulation there is no useful signal received by the antenna. The transmitted signal is made of random OFDM symbols. The OFDM signal has a PAPR of about 10 dB. The output power of the amplifier is set to 20dBm. The parameters used for the models described in Sect. 3.2 are:

- The DACs and ADC have a resolution of 16 bits. Their maximum Integral Non Linearity (INL) is set to a level of 2 Least Significant Bit (LSB), their maximum Differential Non Linearity (DNL) is 0.3 LSB. The maximum output peak-to-peak voltage of the DACs is 5.6 V and the maximum input peak-to-peak voltage of the ADC is 0.3 V.
- The phase noise is characterized by a −110 dB noise floor and a 2-order $1/f^3$ filter.
- The gain of the PA is 10 dB, its 1 dB compression point is 32 dBm and its third order interception point is 40 dBm. The parameters chosen for the Saleh model are $\alpha = 4.5$ and $\beta = 1.1$.
- The gain of the LNA is 10 dB, its 1 dB compression point is −10 dBm and its third order interception point is 0 dBm. Its noise output is at a power of −90 dBm. This noise is taken as the receiver's noise floor.

Simulations highlight the influence of the transmitter noise on performances. Indeed, an all-analog cancellation system as the one presented by [8] is designed to be able to cancel the transmitter's noise included in the self-interference. A hybrid system like ours cannot remove any noise as transmit (x1) and mirrored (x2) paths are uncorrelated. This result was then expected. It also appeared that in our case, the phase noise could be cancelled as we included in the simulation the fact that the phase noises brought by all our mixers was the same but only with different delays. This hypothesis is justified by the fact that mixers use the same local oscillator.



(a) without quantization (b) with 16 bits DAC quantization

Fig. 4. Simulation results

The simulations show that the transmitter noise is by far the most important limiting factor in this architecture, as the system will easily exceed the 100 dB of cancellation when no quantization effects is considered. However, the cancellation is clearly limited by quantization when it is activated. Indeed we can see on Fig. 4 that the signal will not decrease under around −50 dBm after DSIC.

When assuming uniform distribution of quantization error between $\left[-\frac{q}{2}, \frac{q}{2}\right]$, the formula of quantization noise power is given by:

$$QN = \frac{q^2}{12R} \tag{8}$$

Where q is the quantization step. R is the impedance which is 50 ohms. With 16 bit resolution DAC and 5.6 V peak-to-peak voltage, the formula gives an output noise power in all the DAC bandwidth equal to −75 dBm. In the simulations and with the error distribution, the output power is greater and equals to −70 dBm. If we had INL and DNL imperfections, this power would further increase up to −62 dBm.

Then we have to consider the fact that this noise power evolves along the RF chain. On the main transmitter, it is amplified by the PA, then attenuated by the circulator isolation (which is of about 17 dB, Fig. 2), and then amplified again by the LNA. On the auxiliary transmitter chain, the link budget is different as the circulator is replaced by the coupler (10 dB instead of −17 dB). Figure 5 shows both transmitter noise levels along the transmitter receiver path. Both transmitter signals are also included.

We can also notice in Fig. 4. (a) that the HSIC would not reduce the self-interference below about −55 dBm either, even without quantization. This limitation must be due to

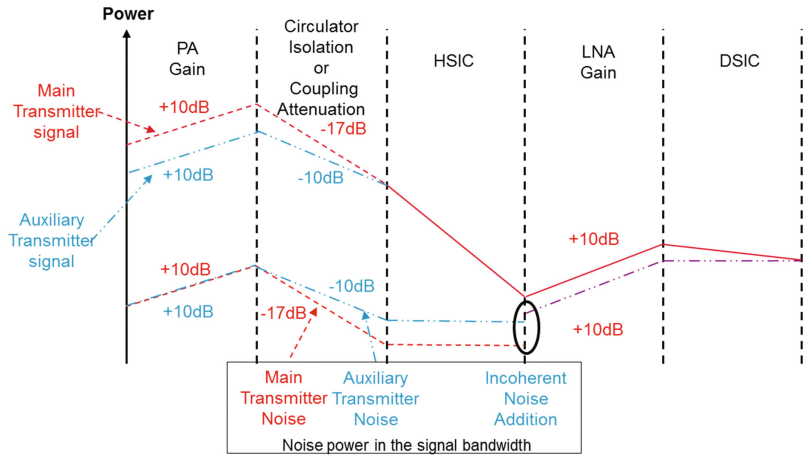


Fig. 5. Evolution of the power versus different RF components (without variable RF gain)

the non-linear distortions of the signal that are not canceled by the HSIC. Indeed, when calculating the power of the difference between the output of the PA and the linearly amplified signal, we get −38 dBm. That power is then attenuated by the circulator of 17 dB which gives −55 dBm and explains the results. Note that the auxiliary transmitter is used at a lower power level so generates less non-linear terms.

4 Simplified Hardware Implementation

In order to understand the effect of the transmitter noise and non-linearity, a simplified hardware implementation has been done using generated signals. It can be considered as a first step to evaluate HSIC performances using real life implementation.

4.1 Overview

The implementation is based on a Red Pitaya [14] board supporting two transmitters and one receiver all synchronized. This board is connected to a personal computer for the transmitted data flow and off-line evaluation. Additional connected RF components complete the demonstration. The useful transmitted baseband signal is digitally transposed on an IF and then converted in the analog domain. An amplifier used in a non-linear zone creates non-linearities. The experimentation is realized in a controlled environment. The antenna and the circulator are emulated by a loss which is approximately equal to −20 dB. After that the auxiliary transmitted signal is added thanks to a 10 dB coupler. For the demonstration, a 3 dB splitter is added to measure the performance and the HSIC. Then, a LNA with variable attenuator is inserted to adapt the input power level to the next amplifier (Fig. 6).

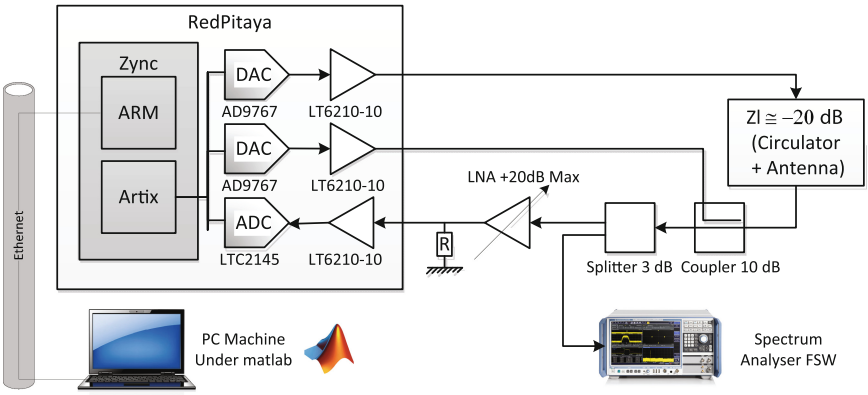


Fig. 6. Testbed overview

4.2 Red Pitaya Board

The Red Pitaya unit is an embedded oscilloscope and signal generator running on Linux operating system. It includes Radio Frequency signal acquisition and generation technologies, FPGA, Digital Signal Processing and CPU processing. The original Red Pitaya board is designed on a Zynq-7010 component and supports two transmitters and two receivers.

The board has been customized with a Zynq7020 instead of the Zynq7010. It contains a dual core ARM Cortex A9 and a Xilinx Artix-7 FPGA with 74 K programmable logic cells.

This board has also two analog outputs and two analog inputs with sampling converters working at 125 MHz. DAC and ADC sample signals at 125 MHz over 14 bits. Table 1 summarizes the main parameters of the hardware elements.

Table 1. Main parameters of the Red Pitaya board.

Functions	Components	Main characteristic
Digital	Zynq 7020	ARM dual core Cortex A9, ARTIX 7
2 DAC	AD9767	14 bits 125 MHz over ±1 V
ADC	LTC2145	14 bits 125 MHz over ±1 V
Amplifier	LT6210-10	Low Noise Op 0.95nV/$\sqrt{Hz}$ Amp Family 1.6 GHz

4.3 Waveform Definition

An Orthogonal Frequency Division Multiplexing (OFDM) waveform has been used at the transmitter. It spans over 20 MHz of bandwidth and it is transmitted on an IF of around 20 MHz.

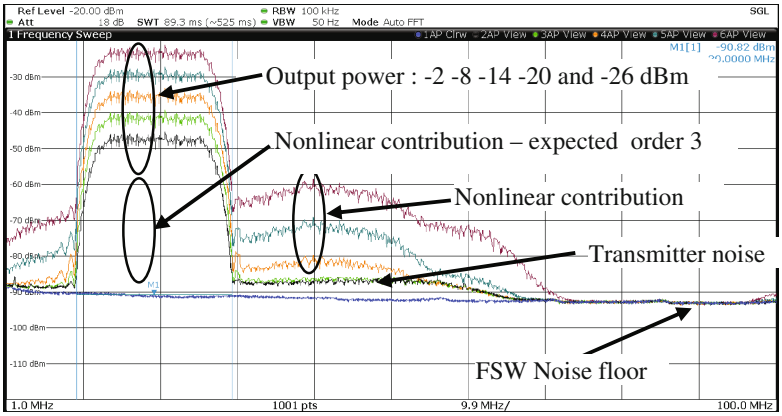


Fig. 7. Transmitted spectrum for different output powers

4.4 Transmitter Noise and Non-linearity

Figure 7 shows the spectrum at the output of the amplifier of the hardware demonstrator. Different output powers are transmitted from −2 dBm down to −26 dBm by 6 dB steps to estimate the nonlinear contributions and transmitter noise.

4.5 Performances

The following figure shows the spectrum at the output of the amplifier and after the HSIC more exactly after the splitter (Fig. 8).

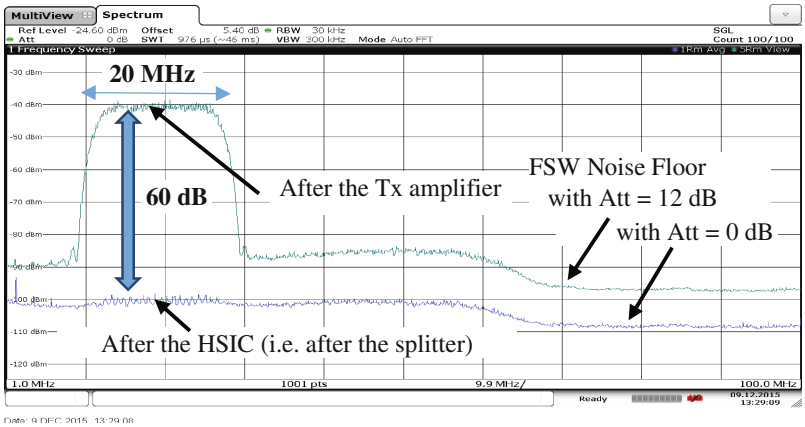


Fig. 8. HSIC performances

The isolation and the HSIC canceller reduce the self-interference by about 60 dB over the 20 MHz band. The DSIC performances is not showed as it cannot reduce self-interference lower than the transmitter noise received after the ADC. The transmitter is the critical parameter for high performances. The next section proposes an evolution of the architecture to reduce the effect of the transmitter noise.

4.6 RF Architecture Evolution

Several issues have been identified thanks to the theoretical study and the practical measurements. First of all, the transmitter noise must be as low as possible. Three solutions could be proposed:

(a) To add a direct RF path from the main transmitter as in the classical approach,
(b) To increase the oversampling to spread the DAC noise over the overall bandwidth and
(c) To use a variable gain on both transmitters to get same level of noise power at the output of the analog canceller.

Moreover, it is useful to add a controlled attenuator before the LNA. This avoids saturation of the LNA and ADC during the calibration phase when transmitted signals are very strong (compared to the received signal coming from the antenna) (Fig. 9).

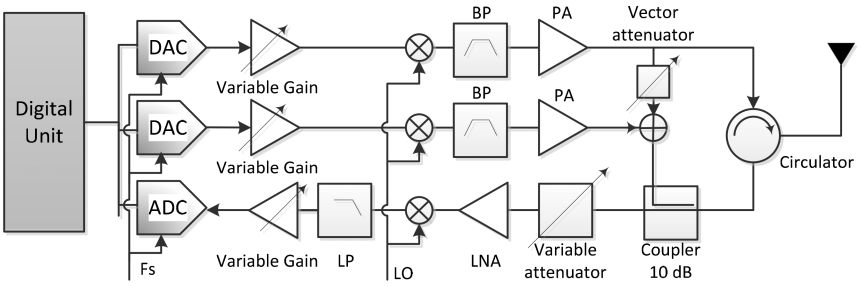


Fig. 9. Architecture evolution

5 Conclusion and Perspective

Based on a flexible RF architecture which is able to switch between FDD MIMO transceiver and IBFD single ended transceiver, we evaluate self-interference cancellation techniques taking into account major RF impairments. As expected, the performance of the transmitters is critical in the proposed architecture as both transmitters have a strong impact on the first analog canceller. The transmitter noise and non-linearity effects are critical parameters. With the proposed architecture, the transmitter noise should be reduced as much as possible. Oversampling is a possibility along with a reduction of the transmitted bandwidth. A trade-off needs to be found between cancellation performance and transmission bandwidth related to full-duplex bit rate. The non-linearity effect is also

important but its impact can be compensated. Nevertheless simulations show that non-linear cancellation is very complex if we suppose that both RF transmitters work in their nonlinear zone. This work has been completed by practical measurements to validate the model and increase our understanding. To conclude, direct analog cancellation path from the main transmitter to the receiver seems to be unavoidable to provide high level of interference cancellation. Future work should investigate an architecture compromise that is based on multiple transmitters (a main transmitter for signal output and a mirror transmitter for signal cancellation) combined with a very simple RF canceller. This new proposed architecture seems to be a good trade-off between the complex solution of Stanford [8] and our first architecture.

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