A Flexible 5G Receiver Architecture Adapted to VLSI Implementation

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Abstract. A flexible data frame structure adapted to 5G operations and designed to support high bandwidth pipes or sporadic traffic is described. The frame structure imposes to consider receiver architectures that are adapted to orthogonal frequency division mutliplexing (OFDM) for structured synchronous traffic and alternative flexible asynchronous waveforms such as filterbank multicarrier (FBMC) for sporadic traffic. OFDM and FBMC receivers are reviewed and a new flexible receiver architecture is then proposed and described. The design of the new architecture is centered on a memory unit complemented with co-processor units improving the flexibility of the digital signal processing operations of the receiver. The architecture is particularly adapted to application specific integrated circuit. The throughput imposed on the memory and the associated data receiver bus has been evaluated. The evaluation concluded that the throughput is suitable for very large scale integration implementations.

Keywords: FBMC · OFDM · LTE · 5G · Architecture

1 Introduction

So far, the appetite for broadband service has fueled the development of mobile cellular networks. Mobile communications started with wireless real time voice communications in the first and second generations of cellular systems (1G and 2G) to provide reliable voice connectivity everywhere. It was then followed by internet data connectivity in the third generation (3G) when the adoption of laptop computers became widespread to bring internet on-the-go. Finally, the advent of the smart-phone accelerated the demand for high bandwidth with the world information accessed at the tip of everyone's finger everywhere at anytime. Therefore, the aim to deliver high-bandwidth pipes has logically been the main driver for the current fourth generation (4G) also called Long Term Evolution (LTE) and LTE-Advanced (LTE-A).

In order to maximize spectral efficiency, strict synchronization and orthogonality between users within a single cell is imposed by LTE and LTE-A standards. However, sporadic traffic has emerged as an important service for future generations of cellular networks (5G). Machine Type Communications (MTC)

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D. Noguet et al. (Eds.): CROWNCOM 2016, LNICST 172, pp. 487–497, 2016.
DOI: 10.1007/978-3-319-40352-6_40

devices of the Internet of Things are expected to inherently generate sporadic data traffic to the network and should not be forced to be integrated into the constrained synchronization procedure of LTE-A in order to limit signaling overhead. Furthermore, a previously unforeseen mechanism designed to save battery usage of the handset also called fast dormancy has resulted in significant control signaling growth. This mechanism causes the user equipment (UE) to go into a deep sleep mode and break any connection to the network. When the UE changes back to an active state the mobile has to go through a complete synchronization procedure again. This phenomenon is another significant source of sporadic traffic on the network [1].

Furthermore, because spectrum is scarce and expensive, its utilization should be as optimal as possible. However, the nature of the sporadic traffic causes significant fragmentation. Therefore carrier aggregation will be implemented to achieve much higher rates by dynamically aggregating non-contiguous frequency bands [2]. However, legacy LTE-A imposes generous guard bands to other legacy networks to satisfy spectral mask requirements because of the poor frequency localization of OFDM.

Therefore relaxed synchronization and access to fragmented spectrum have been considered as key parameters for future generations of wireless networks [1,2]. This requirement of spectrum agility has encouraged the study of alternative multicarrier waveforms such as filter bank multicarrier (FBMC)to provide better adjacent channel leakage performance without compromising spectral efficiency [3].

So far, few studies have been realized to evaluate the architecture trade-offs of hardware implementations of FBMC transceivers. An implementation of a software defined radio platform has been described in [4]. In [5], a complete design and prototyping flow from algorithm specifications to on-board validation and demonstration has been evaluated in the context of 5G using FBMC waveforms. Finally, The authors of [6] demonstrated one of the most achieved concepts with a real time non-synchronous mulituser FBMC transceiver operating over-the-air on fragmented spectrum. All these results have demonstrated the feasibility of prototyping FBMC transceivers with a reasonable level of complexity and are adapted to today hardware platforms. However, coexistence of new asynchronous waveforms with legacy systems (e.g. LTE) should be investigated and architectures adapted to new scenarios should be optimised. The objective of this paper is to propose and evaluate an architecture of implementation suitable to very large scale integration (VLSI) targets (FPGA, ASIC) that could support both OFDM and FBMC receivers.

The paper is organized as follows. First, a review of the so called unified frame structure for 5G is described and the FBMC system model introduced. A current architecture of an FBMC receiver is then analyzed. Finally, a new flexible architecture is proposed and evaluated.

2 Scenario and Model

2.1 Unified Frame Structure for 5G

In order to provide a uniform service experience to users with the premises of heterogeneous networking but also higher data rates, the authors of [1] introduced the concept of the unified frame structure for 5G. The idea is to provide a flexible multi-service solution in an integrated air interface. A frame, divided into different areas of services has been proposed. Four types of traffic have been devised to allow for flexible operation. An example of the proposed frame is shown in Fig. 1: type I and II represent high data rate traffic for video or other high bandwidth services, type I possibly also carries real-time traffic. Type III and IV are dedicated to sporadic asynchronous MTC traffic. Different levels of traffic scheduling have thus been considered: strictly scheduled and organized traffic as already in place in LTE and LTE-A is dedicated to high bandwidth data pipes while sporadic traffic uses contention-like based approaches with random access designed to efficiently enable MTC type payloads (Type III and IV) and bring an efficient solution to the fast dormancy issue.

In order to be efficient, this structure clearly demands to revisit the strict synchronism and orthogonality that prevails in current LTE-A systems. This new requirement leads to rethink the transmission technique and consequently the transceiver structure of the 5th generation of cellular networks.

Alternative waveforms such as UFMC [7], GFDM [8] and FBMC have thus been considered. The motivation of these new waveforms is to keep the flexibility of multicarrier modulations while the frequency response of each carrier is controlled by introducing a filterbank centered on every active carrier and based on the same prototype response. This prototype filter can be selected to minimize adjacent channel interference. As the filtering is embedded in the digital modulation no additional filter is required and more flexibility is obtained.

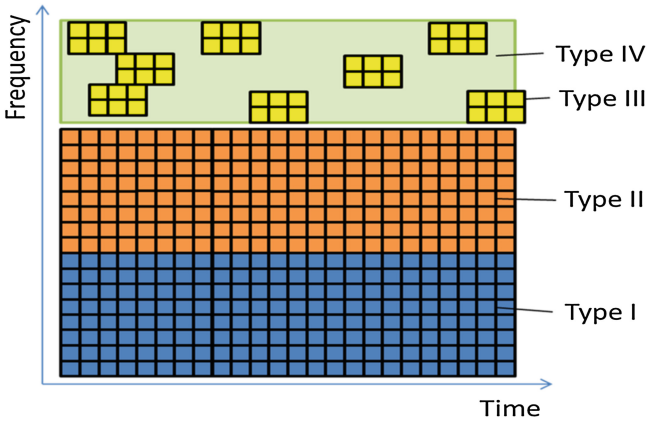

Fig. 1. 5G unified frame structure proposed by [1] (Color figure online)

When considering the unified frame structure, a mix of synchronous (high data rate pipe) and asynchronous traffic should coexist. In this 5G scenario, considering legacy waveforms (i.e. OFDM) for structured synchronous traffic and flexible asynchronous waveforms (i.e. FBMC) for sporadic traffic is very likely. Therefore, an architecture of implementation suitable to VLSI targets (FPGA, ASIC) adapted to both OFDM and FBMC reception should be evaluated.

2.2 OFDM Receiver Architecture

The definition of architectures of OFDM has been widely investigated in the literature [9]. A typical architecture of an OFDM receiver is depicted in Fig. 2. A time domain (TD) synchronization module estimates the start of the multicarrier symbol. The information is used to align a N-point FFT that is processed on the received data every $N+N_{GI}$ samples, where N_{GI} is the size of the guard interval of the OFDM. The N points generated by the FFT are then simultaneously stored to a memory unit for later processing and used by a frequency domain synchronization detector to estimate the carrier frequency offset (CFO).

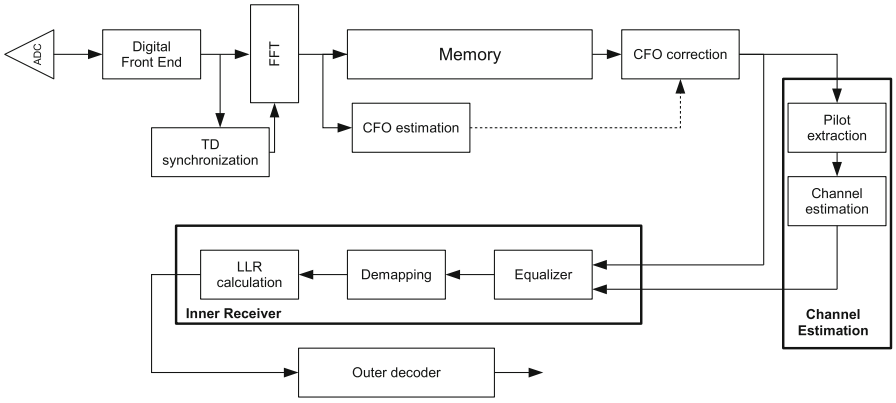

Fig. 2. Typical OFDM receiver block diagram

On the channel estimation datapath, CFO compensation is first performed in the frequency domain using a feed-forward approach. Then, the channel coefficients are estimated on the pilot subcarriers before interpolation for every active subcarrier. Once the channel is estimated on all the active subcarriers the response is stored in a dedicated channel response memory. Depending on the pilot carrier distribution within the time frequency grid, a time interpolation may also be performed. The data buffered in the memory unit are then processed through a one-tap per subcarrier equalizer. Demapping and Log-Likelihood Ratio (LLR) computation complete the inner receiver architecture. A soft-input Forward Error Correction (FEC) decoder finally recovers the originally sent messages.

2.3 FBMC Receiver Architecture

FBMC Review. A multicarrier system can be described by a synthesis/analysis filter bank, i.e. a transmultiplexer structure. The synthesis filter bank is composed of a set of parallel transmit filters. FBMC waveforms utilize a prototype filter designed to give a good frequency localization of the subcarriers. The prototype filter considered in this paper is based on the frequency sampling technique [10]. This technique gives the advantage of using a closed-form representation that includes only a few adjustable design parameters.

The most significant parameter is the duration of the impulse response of the prototype filter also called overlapping factor, K. The impulse response of the prototype filter is given by [10]:

$$h(t) = G_P(0) + 2\sum_{k=1}^{K-1}(-1)^k\, G_P(k)\; cos\left(\frac{2\pi k}{KN}\,(t+1)\right) \tag{1}$$

where $G_P(0..3) = \left[1,\ 0.97195983,\ \frac{1}{\sqrt{2}},\ 1 - G_P(1)^2\right]$ for an overlapping factor of $K = 4$ and N is the number of carriers. The larger the overlapping factor K, the more localized the signal will be in frequency. Adjacent carriers significantly overlap with this kind of filtering. In order to keep adjacent carriers orthogonal, real and pure imaginary values alternate on successive carrier frequencies and on successive transmitted symbols (Offset-QAM modulation is used) for a given carrier at the transmitter side. The well-adjusted frequency localization of the prototype filter guarantees that only adjacent carriers interfere with each other. This allows for a more flexible operation than OFDM for Frequency Division Multiple Access (FDMA), i.e. non synchronous flexible frequency division multiple access.

Most of the published receiver architectures are based on PolyPhase Network (PPN) receivers [10]. In this scheme, the filterbank process is applied in the time domain before the FFT using a polyphase filter. It reduces the size of the FFT but makes the receiver less tolerant to large channel delay spread or synchronization mismatch of the FFT. Therefore, this strategy is not well adapted to the reception of non synchronous users. In [3], the authors describe a high performance receiver architecture denoted FS-FBMC (Frequency Spreading FBMC). One advantage of this architecture comes from the fact that time synchronization may be performed in the frequency domain independently of the position of the FFT [3]. This is realized by combining time synchronization with channel equalization. Moreover, good performance for channel exhibiting large delay spread is achieved [3]. This asynchronous frequency domain processing of the receiver provides a receiver architecture that allows for multiuser asynchronous reception particularly adapted to the envisaged scenarios.

FS Based Receiver. FBMC waveforms are expected to be spectrally more efficient than OFDM when relaxed synchronization between users is considered. Therefore, a preferred architecture for FBMC receivers should be able

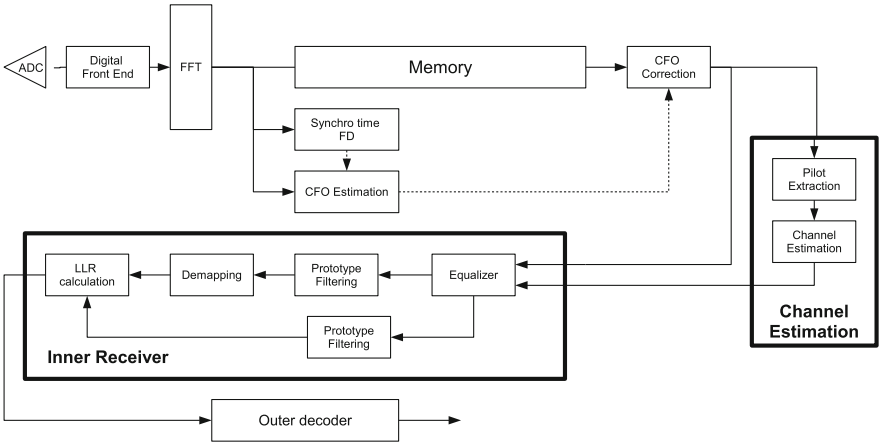

Fig. 3. Typical FBMC receiver block diagram [6]

to efficiently demodulate the signal in the frequency domain without a priori knowledge of the FFT timing alignment (i.e. the location of the FFT block) [6]. A FBMC receiver architecture based on this criteria is given in Fig. 3. A free-running FFT of size KN is processed every blocks of $N/2$ samples generating KN points that are stored in a memory unit for later processing. In parallel a frequency domain synchronization detector detects the start of burst and directly estimates the CFO at the output of the FFT. On the channel estimation datapath, CFO compensation is first performed in the frequency domain using a feed-forward approach. Then, as for OFDM, channel coefficients are estimated on the pilot subcarriers before being interpolated on every active subcarrier. Once the channel is estimated on all the active subcarriers the response is stored for each user in a dedicated channel response memory. The data buffered in the memory unit is then processed through a one-tap per subcarrier equalizer before filtering by the FBMC prototype filter. Demapping and Log-Likelihood Ratio (LLR) computation complete the inner receiver architecture. As far as the LLR computation is concerned, processing is slightly different for FBMC than OFDM. Indeed, in case of a FS-FBMC architecture based receiver, the computation of the LLR associated to a bit from an observation symbol is a function of $2K-1$ channel coefficients [3].

3 Hardware Architecture of a Flexible FBMC Multicarrier Receiver

3.1 Description

Considering the envisaged scenario for 5G described in Sect. 2, a flexible receiver architecture should be able to dynamically receive legacy LTE signal and asynchronous 5G waveforms. An architecture adapted to the aforementioned unified

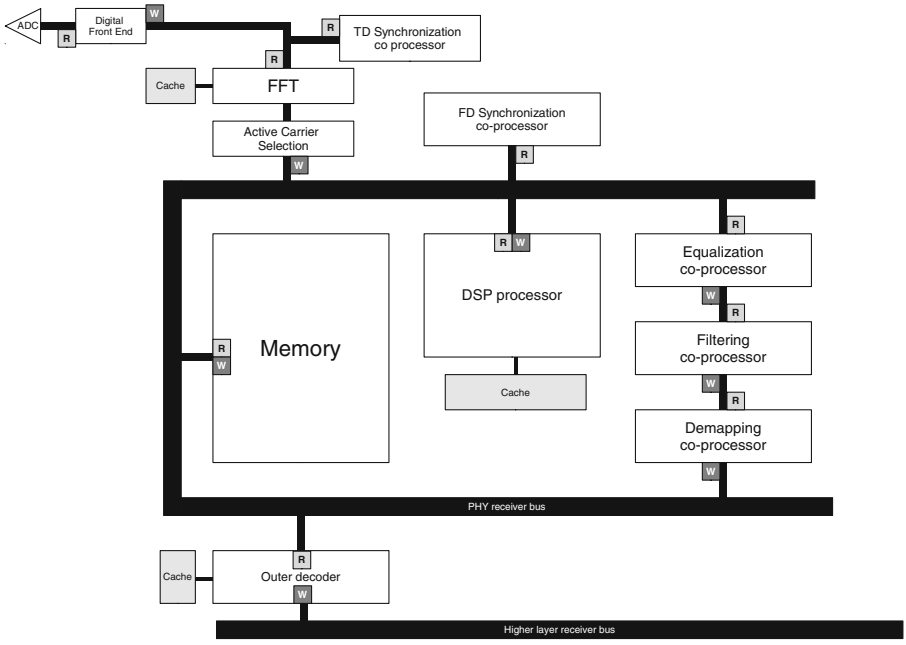

Fig. 4. Flexible architecture adapted to 5G unified frame structure

frame structure has been depicted in Fig. 4. The proposed architecture considers dynamic support for both OFDM and FBMC.

A central memory unit dedicated to the physical layer (PHY) is at the core of the flexible receiver. A set of co-processor units are able to access this central memory through a high speed PHY receiver data bus. These modules include a FD synchronization co-processor (Fig. 4), a FFT co-processor (FFT and Active Carrier selection in Fig. 4), a DSP processor, an Equalization/demapping co-processor (Equalization, filtering and demapping co-processor in Fig. 4) and an Outer decoder processor. A control plane dedicated to transfer control information has been omitted on purpose in Fig. 4 to improve clarity of the figure. The information transiting through the control plane is of relatively low throughput.

The sampled signal received at the analog-to-digital converter is first conditioned by the digital front end to the appropriate sampling frequency into a baseband signal. A TD synchronization processor is at the output of the digital front end and determines the beginning of the burst when in OFDM mode. The module runs in parallel to the FFT module that can either be controlled by the TD synchronization module (when in OFDM mode) or be in free running mode. Appropriate control sets the size of the FFT (N when in OFDM mode or KN when in FBMC mode). The FFT module is followed by an active carrier selection module that selects the active carriers and can write the result to the Memory unit through the PHY receiver bus. In the case of the 20MHz LTE mode, 1201 carriers are typically selected out of the 2048 points at the output of the FFT.

A FD synchronization co-processor can then read the blocks of data samples at the output of the FFT through the PHY receiver bus in order to either estimate CFO when in OFDM mode or estimate CFO and detect start of burst when in FBMC mode. FD synchronization output control signals are then shared through the control plane bus.

Equalization, demapping and LLR computation are hard-wired functions assuming a data-flow architecture. Compared to classical OFDM processing, FBMC includes an extra frequency domain filtering module. The module is therefore bypassed when in OFDM mode. Once the demapping is done, LLR values are written back to the shared memory for further processing by the Outer decoder. As mentioned in the previous section although slightly different demapping follows is very similar process between FBMC and OFDM.

A dedicated digital signal processor (DSP) that can access to its dedicated cache memory has been considered for processing operations such as deframing, pilot extraction and channel estimation. This choice has been driven by the amount of control that these operations required which are therefore more adapted for implementation by an embedded software processing unit. Finally, a dedicated outer module with its internal (cache) memory completes the receiver. The output of the outer decoder is connected to the higher layer bus.

The design of such an architecture where the processing data path is centered on a memory unit has been driven by mainly two motivations. First, the architecture gives more flexibility to the sequencing of the different co-processing units, second and foremost it avoids unnecessary duplication of memory banks. This latter advantage is particularly beneficial for ASIC implementation as large memory banks scale well when using submicron technologies. The main drawback however comes from the constraints that are imposed on the memory and high speed data bus throughput as all the samples written to or read from the memory have to go through the same interface (i.e. the PHY receiver bus). The memory bus throughput has therefore been estimated in the following section to evaluate the relevance of the proposed architecture.

3.2 Memory Bus Throughput Estimation

In order to estimate the constraints that have been put on the PHY receiver bus, an analysis of the throughput has been realized for this architecture. Throughput has been first evaluated analytically for the key modules of the receiver (FFT and the equalizer) for OFDM and for FBMC reception. The results have been summarized in Table 1 in samples per second. The following parameters have been introduced: F_{CS} refers to the frequency spacing between the carrier of the multicarrier modulation, N_a, the number of active carriers, m the modulation order, γ is the ratio of reference over data signal. In the case of the LTE 20MHz mode, γ is equal to 4.76 % or 0.0476.

At the input of the FFT, the data throughput is the same when the receiver receives OFDM or FBMC signals and is equal to the carrier spacing times the number of carriers in samples per second. Typically, for the worst case of LTE, the 20 MHz mode, carrier spacing is equal to 15kHz and N to 2048 points.

Table 1. Analytic sample throughput at the memory bus

		OFDM	FBMC
FFT	Input	$N_{FFT}F_{CS}$	NF_{CS}
	Output	$\frac{N}{N+N_{GI}}NF_{CS}$	$2KNF_{CS}$
	Active carriers selection	$\frac{N}{N+N_{GI}}N_aF_{CS}$	$2KN_aF_{CS}$
Equalizer	Input	$\frac{N}{N+N_{GI}}N_aF_{CS}$	$2KN_aF_{CS}$
	Output filtering	$\frac{N}{N+N_{GI}}N_aF_{CS}$	N_aF_{CS}
	Output demapper (2^m-QAM)	$mN_a\frac{N}{N+N_{GI}}F_{CS}$	mN_aF_{CS}
DSP	Input	$\gamma\frac{N}{N+N_{GI}}N_aF_{CS}$	$\gamma 2KN_aF_{CS}$
	Output	$N_a\frac{N}{N+N_{GI}}F_{CS}$	$2KN_aF_{CS}$

In this case, the input throughput at the FFT is equal to $30.72Msamples/s$. For OFDM, the FFT output average throughput is then divided by the ratio between N and $N + N_{GI}$ as the guard interval is removed. Then active selection further reduces the throughput by N_a/N. The output of the FFT module is then used as an input to the equalizer, LLR calculation increases the throughput by the modulation order m. For FBMC, when FS-FBMC is considered, the FFT output throughput is however multiplied by $2K$ and therefore significantly increased. Similarly to OFDM, active carrier selection reduces the throughput by N_a/N. The output of the FFT module is also used as an input to the equalizer, where the throughput is divided by $2K$ once the prototype matched filtering is applied. Throughput is then increased as per OFDM by the modulation order m after LLR calculation. The throughput of data processed through the DSP module essentially consists of the channel estimation and interpolation. The output of the FFT is read on the pilot tones only and input throughput is therefore equal to the throughput of the FFT output (after active carriers selection) scaled by γ for both OFDM and FBMC. Then channel state information is interpolated and output for every active carriers. Output throughput is thus equal to the equalizer output throughput of the FFT after active carrier selection.

A numerical application for the LTE $20MHz$ mode has then been derived to evaluate the throughput of data at the bus and summarized in Table 2. As throughput is also dependent on the finite precision of the registers implemented in the receiver function, the following assumptions have been made: the input of the FFT is assumed to be a complex 12-bit input signal. Its output is assumed to be on 16 bits because of the FFT bit growth. Then, input to the equalizer includes both FFT output and Channel state information on 16 bit registers. Finally, LLR values are estimated to be sufficient on 6-bit registers. With these assumptions, For OFDM, the PHY receiver bus should sustain an overall write throughput of $1682Mb/s$ and read throughput of $1707Mb/s$. Assuming a 32-bit (resp. 64 bit) transfer bus, this is equivalent to a data bus throughput of $53Mw/s$ (resp. $26Mw/s$) for write operations and $53Mw/s$ (resp. $27Mb/s$) for read operations. This is relatively low when ASIC submicron implementations are considered.

Table 2. Constraint on bus throughput

		System				Quantization		
		OFDM LTE (20MHz)	FBMC (20MHz)			OFDM LTE (20MHz)	FBMC (20MHz)	
FFT	Input	30,72	30,72	Msamp/s	2 x 12	737,28	737,28	Mb/s
	Ouput	28,70	245,76	Msamp/s	2 x 16	918,46	7864,32	Mb/s
	Active Carrier Selection	16,82	144,00	Msamp/s	2 x 16	538,16	4608,00	Mb/s
Equalizer	Input	16,82	144,00	Msamp/s	4 x 16	1076,32	9216,00	Mb/s
	Output Filtering	16,82	18,00	Msamp/s	/	/	/	
	Ouptut (64QAM)	100,91	108,00	MLLR/s	1 x 6	605,43	648,00	Mb/s
DSP	Input	0,80	6,86	Msamp/s	2 x 16	25,63	219,43	Mb/s
	Output	16,82	144,00	Msamp/s	2 x 16	538,16	4608,00	Mb/s
Outer decoder	Input	100,91	108,00	MLLR/s	1 x 6	605,43	648,00	Mb/s
				Total W		1681,75	9864,00	Mb/s
				Total R		1707,38	10083,43	Mb/s
				Total W+R		3389,13	19947,43	Mb/s
			32 bits BUS	Total W		52,55	308,25	Mw/s
				Total R		53,36	315,11	Mw/s
				Total W+R		105,91	623,36	Mw/s
			64 bits BUS	Total W		26,28	154,13	Mw/s
				Total R		26,68	157,55	Mw/s
				Total W+R		52,96	311,68	Mw/s

However, for FBMC implementation and when similar quantization levels as the levels considered for OFDM reception are assumed, the architecture gives an overall aggregated throughput on the PHY receiver bus that is 5.9 times larger for write operations and for read operations. When a 32 bit (resp. 64 bit) data bus is considered, FBMC receptions requires an aggregated throughput of $308Mw/s$ (resp. $154Mw/s$) for read operations and $315Mw/s$ (resp. $158Mw/s$) write operations. The aggregated throughput assuming a 32-bit data bus seems to be in the upper limit of the possibilities available for ASIC submicron technologies, while 64-bit data bus is acceptable. Furthermore, throughput constraints are well balanced between write and read operations.

4 Conclusion

A flexible data frame structure designed to support high bandwidth pipes and sporadic traffic introduced by MTC and fast dormancy has been described. This new requirement imposed by 5G applications has led to consider legacy waveforms such as OFDM for structured synchronous traffic and alternative flexible asynchronous waveforms such as FBMC for sporadic traffic. In order to evaluate an architecture for a flexible receiver adapted to both OFDM and FBMC reception for VLSI targets, OFDM and FBMC receivers have been reviewed. A new type of flexible architecture receiver has then been proposed and described. A memory block combined with a high speed data bus is at the core of the newly proposed architecture. The design of an architecture centered on a memory unit

combined with co-processor units. It improves the flexibility of the digital signal processing operations of the receiver as the sequencing of the processing operations is more flexible. Furthermore, the architecture limits the amount of memory blocks in the design which is particularly beneficial for ASIC implementation. Finally, the throughput on the memory and the associated PHY receiver bus that this new architecture imposes has been evaluated. The paper concluded that the throughput imposed by FBMC reception is almost 6 times bigger for write operations and for read operations in comparison to OFDM reception. Although the difference is significantly high, the maximum estimated throughput is adapted to the constraints imposed by VLSI implementations when a 64-bit bus is implemented even when $20MHz$ bandwidth scenarios are considered.

Acknowledgments. The research leading to these results was supported by the European Commission under grant agreement 671563 (H2020-ICT-2014-2 / ICT-14-2014), Flexible and efficient hardware/software platforms for 5G network elements and devices (Flex5GWare).

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