Modeling of Sigma-Delta ADC with High Resolution Decimation Filter

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Abstract. This paper presents modeling of Sigma-Delta ADC in time domain and frequency domain. Sigma-Delta converters offer high resolution, high integration, and low cost, making them a good ADC choice for applications such as process control and weighing. Analog block of Sigma-Delta ADC consist of integrator, comparator & feedback loop. Analog block provides one bit stream output, which needs to be decimated by digital filter. The digital part consists of filtering and decimation. Proposed technique uses weighted average method for decimation filter to increase the resolution. To understand the various concepts of Sigma -Delta ADC such as noise shaping, over sampling and digital decimation filtering it is required to build frequency domain model, this makes the analysis simpler. Performance is measured in terms of SNR of decimation filter. Synthesizable Register Transfer Level (RTL) code is written for the decimation filter to verify its performance.

Keywords: Over sampling, Noise shaping, Decimation filter.

1   Introduction

The sigma delta conversion technique has been in existence for many years, but recent technological advances now make the devices practical and their use is becoming widespread [1]. In communication system applications, pipelined ADCs and sigma-delta ADCs attract more research efforts. However, the former should be extended to high resolution and the latter to higher bandwidth. The key feature of these converters is that they are the only low cost conversion method which provides both high dynamic range and flexibility in converting low bandwidth input signals.

1.1   Architecture of Sigma-Delta ADC

The basic block diagram of a first order Sigma-Delta ADC is as shown in figure 1. It is comprised of a 1-bit ADC (typically known as a comparator) driven by the output of an integrator that is fed with an input signal summed with the output of a 1-bit DAC fed from the ADC output. Adding a digital low pass filter (LPF) and a decimator to the digital output will create a Sigma-Delta ADC [2].
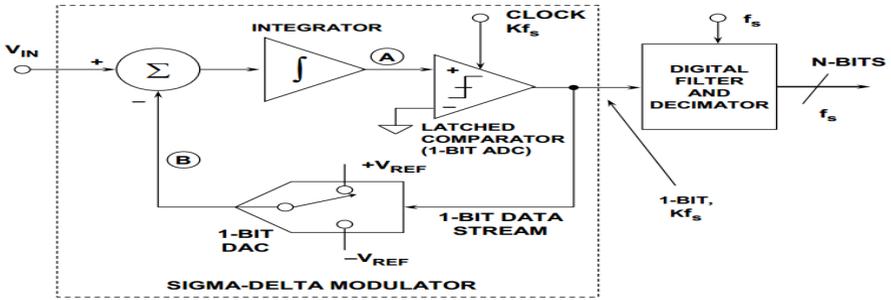
Fig. 1. Block diagram of Sigma-Delta ADC

Sigma-Delta ADC is oversampling ADC. This oversampling results in the two effects. 1) Impact on anti-aliasing filters. 2) Impact on quantization noise.

2   Frequency Domain Modeling

2.1   Modeling of Modulator

In the frequency domain model, the basic approach is to model the transfer functions and hence the frequency responses of the modulator and decimation filter. Over Sampling Ratio is the Ratio of Sampling Frequency to Nyquist Frequency. For example, arbitrarily choosing the OSR as 100 and the Input Frequency as 100 Hz, the Nyquist Frequency is 200 Hz. The OSR of 100 implies the Sampling Frequency is 20000 Hz. Quantization Noise Spectrum is Flat from D.C to Sampling frequency of 20000 Hz (White Noise)and the total Noise Power= $\Delta^2/12$ (Obtained by assuming that the quantization error is uniformly distributed between $-\Delta/2$ to $+\Delta/2$). Where Δ= step size = $1/(2^n-1)$. (Assuming Full Scale output voltage of 1V), Choosing n=1 bit, $\Delta=1$, resulting Noise Power = 0.0833. Uniformly spread this power from 0 to 20K Hz, We obtain the amplitude of the noise spectrum as 0.002041.

The modeling of the modulator mainly depends on its noise transfer function. The desired Noise Transfer function is s/(s+a), where 'a' is half of Sampling Frequency (Fs/2=10000).

Block diagram simplification results in the noise transfer function as 1/(1+I(s)). Where, I(s) is the transfer function of the integrator. The integrator transfer function will be a/s = (10000/s). Signal transfer function is given by I(s)/(1+I(s)) where I(s) is the integrator transfer function , Substituting the integrator transfer function obtained, we get the signal transfer function as a/(s+a). Multiplying the Signal and Noise with the Signal and Noise Transfer Functions respectively, we obtain the Signal and noise output from the Modulator as shown in figure 2.
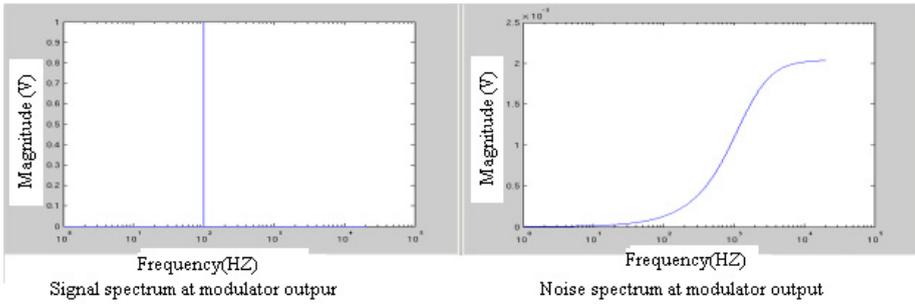
Fig. 2. Signal and Noise spectrum at the Modulator Output

Noise spectrum at modulator output shows that noise added to the input signal is moved to the higher frequencies making the band of interest having lesser noise, this technique is called noise shaping it can be changed by modifying the noise transfer function. This noise shaping results in increased SNR compared to other ADC's.

2.2   Modeling of Decimation Filter

Filtering noise which could be aliased back into the baseband is the primary purpose of the digital filtering stage. Its secondary purpose is to take the 1-bit data stream that has a high sample rate and transform it into a high resolution data stream at a lower sample rate. This process is known as decimation. Essentially, decimation is both an averaging filter function and a rate reduction function performed simultaneously. The output of the modulator is a coarse quantization of the analog input. However, the modulator is oversampled at a rate that K times higher than the Nyquist rate. High resolution is achieved by averaging over K data points to interpolate between the coarse quantization levels of the modulator. The process of averaging is equivalent to lowpass filtering in the frequency domain. With the high frequency components of the quantization noise removed, the output sampling rate can be reduced to the Nyquist rate without aliasing noise into the baseband. The Decimation Filters impulse response is either a rectangular or triangular function. Therefore, its Frequency response is a Sinc or $Sinc^2$ function respectively .The Bandwidth of these filters are selected in such a way that the input signal is well inside the pass-band of these filters. The Signal and Noise Output Spectrum from the Modulator are multiplied by the frequency response of the decimation filter to obtain the final Signal and Noise Outputs. Since the Signals are already in the frequency domain, just squaring and adding the amplitude gives the power of each signal. The Power of the Signal and noise is calculated and the SNR is evaluated as the 10*log10 (signal power / noise power).

2.3   Comparison of Theoretical and Obtained Results

We plot the Ideal SNR and the Obtained SNR vs. the OSR for both the first order and second order decimation filters.
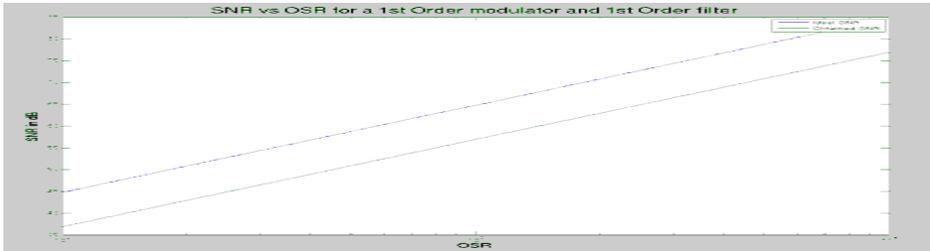

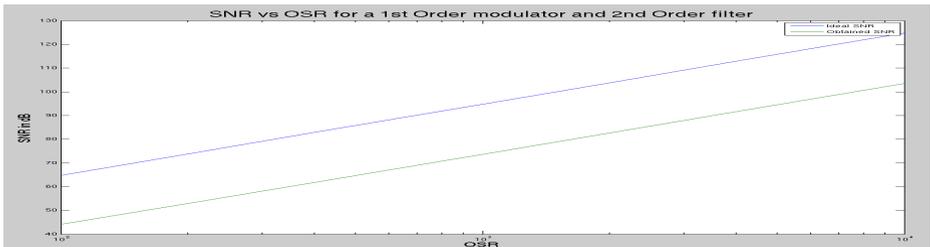**Fig. 3.** SNR vs. OSR for a first order decimation filter

Fig. 4. SNR vs. OSR for a second order decimation filter

In all cases, we observe that there is an offset between the ideal and the obtained SNR. This is because of the attenuation caused to the input signal by the decimation filter which we had not considered in our derivation of the Ideal SNR equation.

3   Time Domain Modeling

A sinusoidal input of 10Hz and sampling frequency of 80 KHz is chosen. Therefore the OSR is 4000. Modulator is modeled as shown in figure 1, The integrator is an ideal integrator whose output is the present input plus the previous output. The comparator is a simple threshold device which outputs a high value if its input is positive and a low value otherwise. The DAC outputs a value of Vref if its input is high and a value of –Vref otherwise [4]. The time domain output of the modulator is shown in figure 5 .We observe that the time domain output has more ones when the input has a high magnitude and the output has more zeros when the magnitude of the input is low also, when the input voltage is close to midscale, we see an equal number of ones and zeros [5].
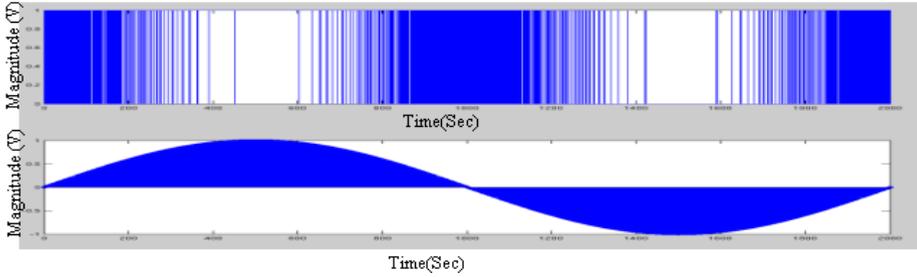
Fig. 5. Time domain output of the modulator

3.1 Time Response of First and Second Order Decimation Filter

The first order filter has a rectangular impulse response, i.e, its output is an average of the previous N inputs where N is the number of taps of the filter. This is decided by the decimation rate. Usually the value of N is chosen in such a way that the output rate is twice or four times the Nyquist rate. The rectangular impulse response results in a Sinc frequency response [5]. The bandwidth of this filter is 40Hz. The bit stream obtained from the modulator is filtered using the first order filter. The second order filter has a triangular impulse response, i.e. its output is a weighted average of the previous N inputs where N is the number of taps of the filter. The triangular impulse response results in a $Sinc^2$ frequency response [5]. The bandwidth of this filter is 80Hz. This is as expected because the second order filter can be visualized and implemented as a cascade of two first order filters.

4 Simulation Results

Time domain model is built in Cadence Virtuoso, switched capacitor integrator is used to model the modulator. Input sine wave of 10Hz frequency and OSR of 4000 is chosen, resulting in 80KHz of Fs, and decimation rate of 1000 is selected. Decimation filter is implemented in Verilog-A model [4]. Input signal, integrator output, filter clock, modulator output and decimation filter outputs are shown in figure 6.
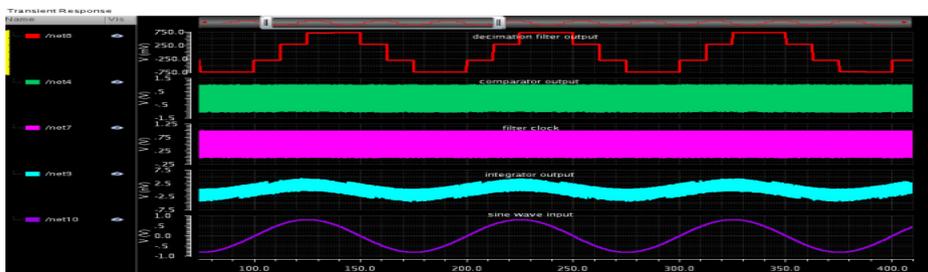

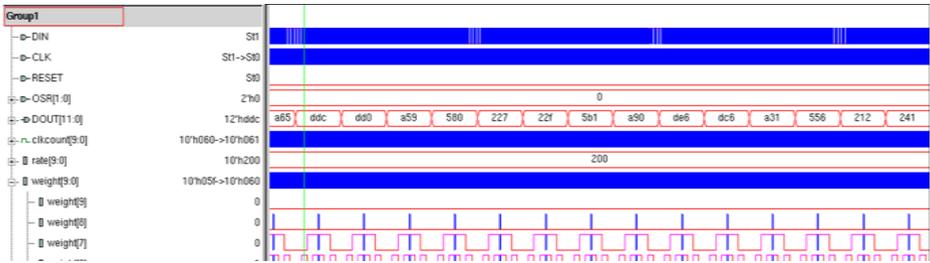**Fig. 6.** Output of the modulator and filter

Fig. 7. ADC output with resolution of 12 bits

In Figure 7, first waveform corresponds to the input of the filter (DIN) or the output of the comparator, second waveform is the clock, third waveform is reset signal which is held at logic zero and fourth waveform is 2-bits programmable OSR, fifth waveform represents the 12-bit digital output corresponding to the analog input and other signals are the intermediate signals which helps in debugging.

5   Conclusion

We initially built models of the Sigma-Delta ADC in the frequency domain. We compared the SNR results that we obtain from the frequency domain model with the ideal SNR that we get from the equations that we have derived for various orders of decimation filters and observed that the obtained values were in good agreement with the theoretical values. We also built a time domain model of the Sigma-Delta ADC in Matlab as well as in Cadence Virtuoso schematic editor. Based on the SNR results that we obtained from the frequency and time domain models, we developed a synthesizable Register Transfer Level (RTL) code in Verilog HDL for the optimum decimation filter and verified its performance. Second order filter with first order modulator gives better performance than first order filter with first order modulator with 12 bits of resolution.

References

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