A New Nanoscale DG MOSFET Design with Enhanced Performance – A Comparative Study

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Abstract. Triple Material (TM) Double Gate (DG) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) with high-k dielectric material as Gate Stack (GS) is presented in this paper. A lightly doped channel has been taken to enhance the device performance and reduce short channel effects (SCEs) such as drain induced barrier lowering (DIBL), sub threshold slope (SS), hot carrier effects (HCEs), channel length modulation (CLM). We investigated the parameters like Surface Potential, Electric field in the channel, SS, DIBL, Transconductance (g_m) for TM-GS-DG and compared with Single Material (SM) DG and TM-DG. The simulation and parameter extraction have been done by using the commercially available device simulation software ATLAS^{TM}.

Index Terms: MOSFET, silicon-on-insulator (SOI), DG, SCEs, Gate Stack (GS) engineering, TM-DG, ATLAS^{TM} device simulator.

1 Introduction

To scale the planar bulk MOSFET into nanometre regime, significant challenges and difficulties come across to control the SCEs. Various new structures have been reported to reduce the SCEs in SOI devices. The DG MOSFET is one of the promising candidates because of its two gates which control the channel from both sides and electrostatically superior to a single gate MOSFET which allows additional gate length scaling due to good control of SCEs [1],[6],[7].

In SOI devices the leakage current (I_{off}) can be controlled by different architectures. The required threshold voltage (V_T) can be achieved by keeping channel un-doped and altering the gate work function. Thus MOSFETs can be fabricated with lightly doped channels resulting in high carrier mobility [8],[10]. The DG MOSFETs also suffer from considerable short channel behaviour in the sub 100 nm regime. A new device structure TM-DG MOSFET is developed to improve the device immunity against the SCEs and therefore improve the device reliability in high performance circuit applications. This new structure gives improving SCEs such as DIBL, HCEs, reducing channel length modulation (CLM). It also improves the drive current, SS, leakage current and g_m. Three different laterally contacted materials with different work function have been taken for gate electrode of the device. Material

V.V. Das and P.M. El-Kafrawy (Eds.): SPIT 2012, LNICST 117, pp. 76–81, 2014.

work functions will be selected in such a way that work function near the source is highest and near the drain is lowest for n-channel MOSFET. As a result, the electric field and electron velocity along the channel suddenly increase near the interface of the two gate materials, resulting in increased gate transport efficiency. The low work function near the drain side reduces the peak electric field and reduces the HCEs when compared to single material gate structure [2], [3], [4], [5].

Day by day the gate oxide thickness t_{ox} is decreasing and approaching physical limits (<2nm), for which quantum mechanical tunnelling induces severe gate leakage current through the dielectric. In our work the high dielectric material taken over thin SiO_2 layer [10], [11], [12]. We investigate the SCEs of TM-DG MOSFET in comparison with the conventional DG MOSFET. We also have taken TM-GS-DG MOSFET with the high dielectric material Si_3N_4.Our results demonstrated that the proposed TM-GS-DG MOSFET exhibits good current characteristics and reduced SCEs such as DIBL, HCEs and CLM compared to the conventional DG MOSFET and TM-DG MOSFET.

2 Device Structure

Schematic structures of TM-DG and TM-GS-DG MOSFET are shown in Fig.1 and Fig.2 with M1, M2, and M3 of gate lengths L_{G1}, L_{G2}, L_{G3} respectively. We have studied only n-type MOSFET in our analysis. The work function for the gate materials is assumed as 4.8ev for SM-DG and 4.8ev, 4.6ev, 4.4ev for TM-DG. The gate length (L_G) =60nm for SM and for TM gate material length ratio (1:1:1) was taken. The channel thickness t_{Si} =10nm and oxide thickness t_{SiO2}=3nm for SM, TM_DG and t_{SiO2}=1nm, t_{Si3N4}=2nm for TM-GS-DG is made in these devices. Source/Drain doping $N_D=10^{20}$ cm^{-3} with variation of channel doping $N_a=10^{15}cm^{-3}$ to 10^{18} cm^{-3} considered.

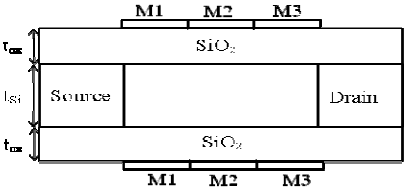

Fig. 1. Schematic of SM and TM-DG MOSFET

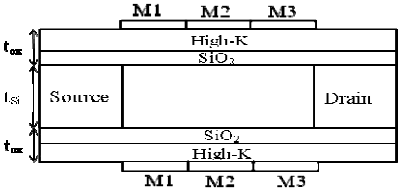

Fig. 2. Schematic of TM-GS-DG MOSFET

3 Simulation

In the simulation the model used comprises the inversion layer Lombardi constant voltage and temperature (CVT) mobility model that takes into account the effect of parallel and perpendicular fields, along with doping and temperature dependent parts of the mobility. The Shockley–Read–Hall and Auger recombination models for minority carrier recombination have been used. Furthermore, we chose Gummel's

method (or the decoupled method), along with Newton's method (or the fully coupled method), to solve the equations included in the CVT model [2], [13].

4 Results and Discussions

In Fig.3., I_{DS}-V_{GS} transfer characteristics on linear scale and log scales for three different device structures have been compared at V_{DS}=10 mV and 1.2 V. We have extracted SS and maximum drain current (Id) for three different structures by changing channel doping which is given in Table 1.

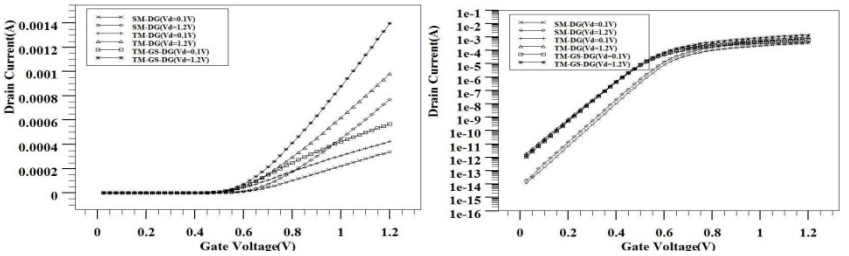

Fig. 3. Simulated drain current I_{DS} as a function of the gate voltage V_{GS} on (a) normal and (b) log scales for three structures at N_A= $1x10^{16}cm^{-3}$

Table 1. Extracted Parameters from Fig.3

Structure		Subthreshold Slope		Max Drain Current	
Model	**$N_A(cm^{-3})$**	**SS ,V_d=0.1V**	**SS , V_d=1.2V**	**I_{d1}(mA) ,V_d=0.1V**	**I_{d2}(mA),V_d=1.2V**
SM-DG	1e+15	62.02	62.34	0.61	1.07
	1e+16	62.04	62.35	0.62	1.08
	1e+17	62.15	62.41	0.56	1.03
	1e+18	62.45	62.12	0.34	0.77
TM-DG	1e+15	67.75	67.99	0.71	1.24
	1e+16	67.74	67.98	0.72	1.25
	1e+17	67.68	67.92	0.66	1.21
	1e+18	66.97	67.43	0.42	0.98
TM-GS-DG	1e+15	65.64	65.73	0.89	1.70
	1e+16	65.65	65.74	0.91	1.71
	1e+17	65.63	65.75	0.84	1.67
	1e+18	65.27	65.51	0.57	1.40

In Fig 4.(a) The sensitivity of SS for different channel doping is demonstrated. The SS is lower for TM-GS-DG than TM-DG. The TM-GS-DG shows a higher drive current than the DG and TM-DG MOSFET with un-doped or lightly body doping ($1x10^{15}$ and $1x10^{16}$) which is examined in Fig. 4(b). The surface potential of the three devices with different V_{GS} and V_{DS} are given in Fig. 5(a). As seen from the figure barrier height for channel carriers at the edge of the source has less change with increase in drain voltage. It is clear from that Fig., the minimum channel potential lies under control of gate voltage.

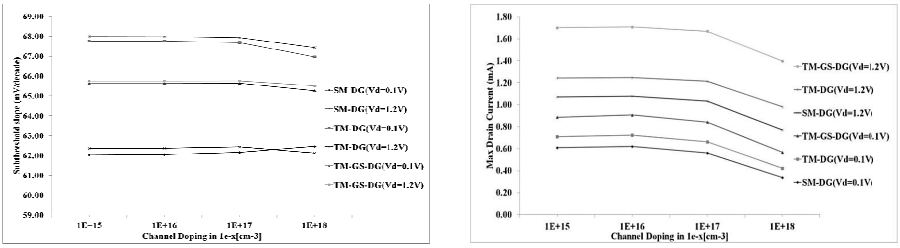

Fig. 4. (a) Variation of SS and (b) maximum drain current for different channel doping (N_A)

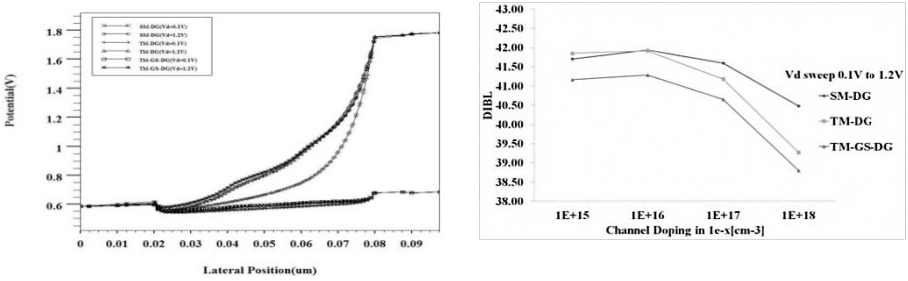

Fig. 5. (a)Surface Potential along the channel for different values of V_{GS} and V_{DS} (b) Variation of DIBL for different channel doping (N_A))

The minimum surface potential extracted as threshold voltage and DIBL are given in Table 2. The sensitivity of DIBL was examined for different channel doping as shown in Fig. 5(b). The figure shows among from the three device structures, TM-GS-DG gives lower DIBL which reduces the SCEs.

Table 2. Extraction of DIBL and Transconductance for different channel doping

Model	$N_A(cm^{-3})$	$V_{t1}(V)$, V_d=0.1V	$V_{t2}(V)$,V_d=1.2V	DIBL	g_{m1} , V_d=0.1V	g_{m2} ,V_d=1.2V
SM-DG	1e+15	0.48	0.02	41.70	1.00	1.86
	1e+16	0.49	0.03	41.94	1.01	1.88
	1e+17	0.50	0.04	41.60	0.92	1.86
	1e+18	0.59	0.14	40.48	0.61	1.68
TM-DG	1e+15	0.43	-0.03	41.85	1.16	1.98
	1e+16	0.44	-0.02	41.91	1.16	2.00
	1e+17	0.44	-0.01	41.18	1.06	1.98
	1e+18	0.50	0.07	39.27	0.71	1.85
TM-GS-DG	1e+15	0.45	0.00	41.17	1.58	2.84
	1e+16	0.46	0.00	41.29	1.60	2.87
	1e+17	0.46	0.01	40.65	1.47	2.84
	1e+18	0.50	0.08	38.81	1.01	2.67

Fig.6. shows electric field in the lateral position of the three device structures with V_{DS} (0.1V and 1.2V). It is clearly visible from that figure the different in the value of work function of the gate material for TM-DG results two additional peaks. The peak value of the electric field at drain side is reduced for TM-GS-DG as compared to SM-DG and TM-DG, which minimises the HCE and impact ionisation. Fig.7 (a) shows the transconductance (g_m) for TM-GS-DG is higher as compared to SM and TM-DG in both the bias voltages. The increment of g_m leads to higher intrinsic gain which gives better RF application.

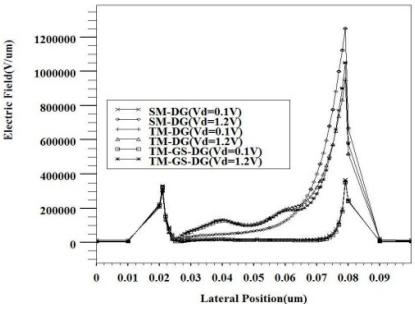

Fig. 6. E. Field for different V_{GS} and V_{DS}

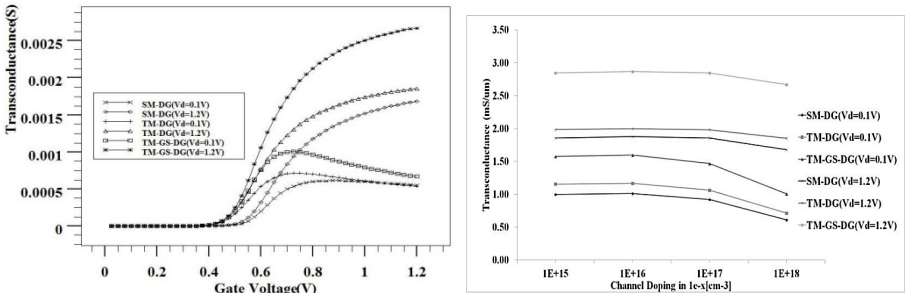

Fig. 7. (a)Variation of g_m as a function V_{GS} for three structures at $N_A = 1x10^{16}cm^{-3}$, (b).Variation of g_m as a function of N_A

The Table 2 is the extraction of g_m for different N_A and the Fig.7 (b) shows the variation of g_m as a function of the channel doping N_A. All three device structures give better g_m for lightly doped channel. The TM-GS-DG shows highest g_m in comparison to SM-DG and TM-DG. The GS engineering provides higher drain current (as shown in Fig.3) because of the reduced EOT which increases the gate capacitance. The increment of drain current increases the transconductance for GS architecture.

5 Conclusion

We provide a thorough investigation of the performance for gate engineering TM and TM-GS double gate MOSFETs as a function of device geometry as well as doping strategies. The design and simulation on NMOS electrical characteristics has been successfully done using commercially available device simulation software ATLAS^{TM}. We can model the SM-DG, TM-DG and TM-GS-DG by altering the material work

function Φ_m and the value of k. The TM-GS-DG shows a better control of gate on the channel that improves the SCEs and also increases the transconductance implies a high dc gain. Reduction of electric field at the drain end indicates a low HCE. From all above simulation results and extracted parameters the TM-GS-DG with less channel doping gives better performance from its counterpart SM-DG and TM-DG.

Acknowledgements. The authors would like to thank the department of Electronics and Telecommunication Engineering, Jadavpur University, West Bengal.

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