

An RGB-LED Driver with Feed-Forward Equalization Used for PAM-4 Visible Light Communication

Bo Xu^{1(⋈)}, Li Wang¹, Jian Kang¹, Cong Qiu², and C. Patrick Yue¹

HKUST-Qualcomm Optical Wireless Lab, ECE Department, The Hong Kong University of Science and Technology, Hong Kong SAR, China bxuag@connect.ust.hk

Abstract. This work proposed a red-green-blue LED (RGB LED) driver based on TSMC 40 nm CMOS process with current regulator structure to drive a 5X5 RGB LED array. By adopting 4-pulse amplitude modulation (PAM-4) scheme and feed-forward equalization (FFE), the simulated driving data rate for each driver can reach 100 Mb/s.

Keywords: LED driver · Visible light communication · 4-Pulse amplitude modulation · Feed-Forward equalization

1 Introduction

With the fast development of wireless communication technology, visible light communication (VLC) has attracted increasing attention from both institute and industry as a significant direction of next generation wireless communication network. Compared with radio frequency (RF) communication, VLC is superior for its wide spectrum, easy implemented, high security, and power efficient especially when combining with extensively existing LED infrastructures. Due to the high output power intensity of LEDs, the signal to noise ratio (SNR) of LED based VLC can be higher than RF communication, which provides advantages for supporting high-order modulation such as carrierless amplitude and phase modulation (CAP) [1], discrete multi-tone modulation (DMT) [2], and pulse amplitude modulation (PAM) [3].

However, most of high-order modulation VLC prototypes are lack of implementation or just composed of discrete components. At the transmitter side, specialized high-speed LED driver is neglected. Traditional current pulse drivers are faced with large rising and falling edge problem when driving a series of LEDs at high switching frequency [4]. In addition, equalization scheme is widely adopted to extend the bandwidth of LEDs and increase SNR.

In this work, we proposed a current regulating red-green-blue LED (RGB LED) driver with feed-forward equalization (FFE) to drive a 5×5 RGB LED array with utilizing PAM-4 scheme. For each color LED series, the VLC driving signal is a non-return-to-zero (NRZ) signal. By combining the three different signals coming from the

² School of Electronic Communication Technology, Shenzhen Institute of Information Technology, Shenzhen, Guangdong, China

three-color LEDs, 4 different current levels can be formed. PAM-4 signal, therefore, is easily realized.

2 System Architecture

As shown in Fig. 1, the whole driver system is consisted of main driver, FFE driver, and light source. To simplify the system architecture, the main driver and FFE driver utilize same structure with different driving current. A 5×5 RGB LED array is used as light source while each color LED array equips with separate main driver and FFE driver. Input VLC data is under NRZ coding and driving red, green, and blue LEDs separately to guarantee the correct superposition in optical domain to form 4 different levels of current which produce final PAM-4 signal. The supplied voltage of LED array is 20 V and the maximum driving current for each LED branch is 60 mA.

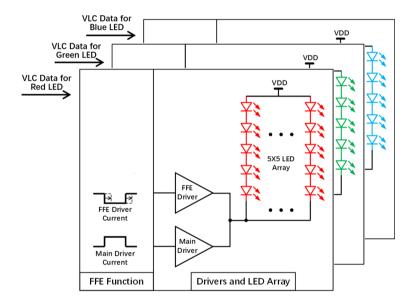


Fig. 1. System architecture of the proposed PAM-4 VLC RGB-LED driver.

2.1 Driver Architecture

Figure 2 merely presents the schematic of main driver while FFE driver employs the same structure and connects to LED array in the same way. The proposed driver is based on current regulator in [5] and simplify the function of timing controller and operational transconductance amplifier (OTA) with a dynamic gate-boosting amplifier (DGB-AMP) in [4]. The rising and falling time of current-pulse driver proposed in [6] is too long to support high speed switching. Besides, longer rising time than falling time will cause shorter high level than low level in OOK modulation, which is the origin of duty circle distortion and will decrease SNR.

In the proposed driver, I_{LED} is given by [5] which is set as 60 mA per branch:

$$I_{LED} = \frac{V_{-,DGBAMP}}{R_1} \tag{1}$$

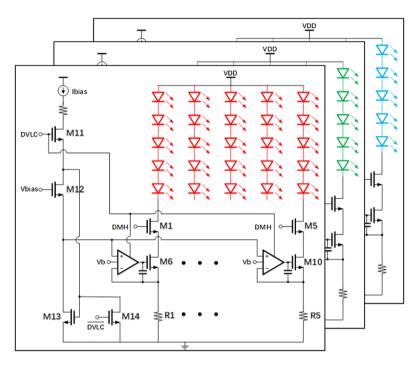


Fig. 2. Schematic of the proposed LED driver with 5X5 RGB LED array.

During the high-level stage of DVLC, the state of enable pulse in DGB-AMP is the same as DVLC which is "ON", thus the gate capacitor of M6–M10 is charged to driving voltage level. When it comes to low-level stage, the enable pulse turns to "OFF" and the charged gate is floating without discharging. The gate signal of M1–M5 (DMH) changes with DVLC synchronously but with different voltage level. At the rising edge, I_{LED} will immediately rise to high-level as the already charged gate capacitor of M6–M10 providing driving voltage to M1–M5, which immensely decreases the rising time. At the falling edge, M14 helps to discharging M13 while M1–M5 turn-off promptly. There strategies will reduce falling time. The capacitor connecting between the gate and source of M6–M10 will remove overshoot of I_{LED} at high-level.

2.2 FFE Implementation

As shown in Fig. 1, the amplitude of both FFE and main driving current is adjustable to maintain a stable output current. FFE driving current derives from main driving current with being properly inverted and delayed. After sent to corresponding FFE driver, the

FFE signal combines with main signal at the end of LED series to form final driving current I_{LED} . The function of FFE is extending the bandwidth by increasing the peak of driving current at rising and falling edges so that the quality of communication can be improved.

3 Simulation Results and Discussion

The simulation verification consists of transient analysis and eye diagram measurement which are performed in EDA tool Cadence with transient noise included. The driver is implemented in TSMC 40 nm process. R-C equivalent model is used as LED load with numerical value of 50 Ω and 200 pF separately. Since the current flowing through resistance connected in parallel with capacitance in LED model changes corresponding with LED light intensity, we utilize this resistance current to represent light signal in eye diagram analysis. Here we just applied random NRZ data as input VLC signal, and more input data pattern such as PRBS-7 could be analyzed in further research.

3.1 Verification of Driver Function

To verify the function of proposed driver, we firstly analyzed the transient waveforms under 10 Mb/s OOK modulation and the result is presented in Fig. 3(a). The maximum driving current is around 60 mA while rising and falling edges changing corresponding with input VLC data. The transient waveforms of three different random 10 Mb/s NRZ data with combined final PAM-4 driving current are shown in Fig. 3(b).

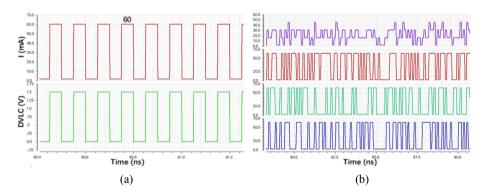


Fig. 3. Simulated transient waveforms of the LED driver with different VLC input data: (a) 10 Mb/s OOK, (b) 10 Mb/s NRZ.

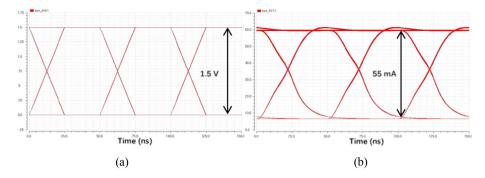


Fig. 4. Simulated eye diagrams for RGB LED single color: (a) input eye diagram of 10 Mb/s NRZ, (b) output eye diagram of 10 Mb/s NRZ.

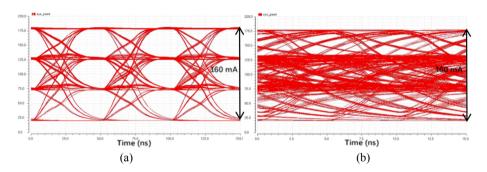


Fig. 5. Simulated PAM-4 eye diagrams for RGB LED with different VLC data rate: (a) 10 Mb/s NRZ, (b) 100 Mb/s NRZ.

Secondly, eye diagram measurement is performed for each color LEDs by analyzing input VLC data and the output current through resistance in LED equivalent model. As shown in Fig. 4(a) and (b), the height of eye diagram for input voltage is 1.5 V while output current is around 55 mA under 10 Mb/s NRZ data.

Lastly, we simulated eye diagrams of RGB LED array drove by combined driving current to verify the accuracy of PAM-4 scheme. The simulation results of random 10 Mb/s and 100 Mb/s NRZ input data are shown in Fig. 5(a) and (b) separately. The height of PAM-4 eye diagram is around 160 mA with exact superpositions of three NRZ signals in Fig. 5(a). In addition, there is no state lacking in this PAM-4 eye diagram. However, it can be noticed that there exists bandwidth limitation in Fig. 5(b) as there almost exists no open eye.

3.2 Verification of FFE

To verify the function of FFE, we simulated PAM-4 eye diagram since there exists evident bandwidth limitation in without FFE case especially for higher frequency. After adjusting both FFE and main driving current to keep 60 mA total driving current, FFE

is employed to the proposed driver. The quality of eye diagram under random 10 Mb/s and 100 Mb/s NRZ data has been improved as shown in Fig. 6(a) and (b). Comparing with Fig. 5, the bandwidth has been extended obviously which is reflected in wider open eyes.

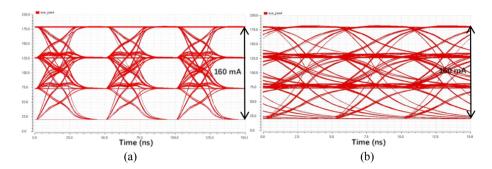


Fig. 6. Simulated PAM-4 eye diagrams with FFE under different VLC data rate: (a) 10 Mb/s NRZ, (b) 100 Mb/s NRZ.

4 Conclusion

In this work, we proposed an RGB-LED driver equipped with FFE to achieve high-speed PAM-4 visible light communication. This driver is based on traditional current regulator structure with decreasing of rising and falling time. Simulation verification utilizing TSMC 40 nm process was applied to prove the feasibility of this driver, which consisted of transient analysis and eye diagram analysis. The results shown that both PAM-4 scheme and FFE are practicable in this driver under up to 100 Mb/s random NRZ data.

Acknowledgement. This work was supported in part by the Research and Development Program in Key Areas of Guangdong Province under Grant 2019B010116002.

References

- Chi, N., Zhou, Y., Liang, S., Wang, F., Li, J., Wang, Y.: Enabling technologies for high-speed visible light communication employing CAP modulation. J. Lightw. Technol. 36(2), 510–518 (2018)
- Cossu, G., Wajahat, A., Corsini, R., Ciaramella, E.: 5.6 Gbit/s downlink and 1.5 Gbit/s uplink optical wireless transmission at indoor distances (≥ 1.5 m). In: 2014 The European Conference on Optical Communication (ECOC), Cannes, pp. 1–3 (2014)
- Li, X., Bamiedakis, N., Guo, X., et al.: Wireless visible light communications employing feed-forward pre-equalization and PAM-4 modulation. J. Lightw. Technol. 34(8), 2049–2055 (2016)
- 4. Kim, J., et al.: A fast-switching current-pulse driver for LED backlight. In: 2009 IEEE International Symposium on Circuits and Systems, Taipei, pp. 1775–1778 (2009)

- 5. Ahn, H., Hong, S., Kwon, O.: A fast switching current regulator using slewing time reduction method for high dimming ratio of LED backlight drivers. IEEE Trans. Circuits Syst. II Express Briefs **63**(11), 1014–1018 (2016)
- 6. Che, F., Wu, L., Hussain, B., et al.: A fully integrated IEEE 802.15. 7 visible light communication transmitter with on-chip 8-W 85% efficiency boost LED driver. J. Lightw. Technol. **34**(10), 2419–2430 (2016)