System Level Performance Analysis of Designed LNA and Down Converter for IEEE 802.11ad Receiver

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Abstract. A low noise amplifier (LNA) operating at millimeter wave (mmWave) frequency and a down converter suitable for IEEE 802.11ad receiver is designed in a 65 nm radio frequency (RF)-CMOS low leakage (LL) process. These designed blocks are integrated in a super heterodyne receiver architecture and the overall performance of the receiver is analyzed. The designed LNA gives a performance metric of 20 dB of gain, 1.7 dB of noise figure (NF) and −7.78 dBm of IIP3. Modified Gilbert cell topology is used for down converter which gives a conversion gain of 1.5 dB from 57 GHz to 66 GHz, input P_{1dB} of −7.8dBm and IIP3 of 8.78 dBm with RF at 57.24 GHz from a 1.2 V supply voltage and a 1Vpp of local oscillator (LO) drive. The obtained IIP3 is 10.08 dB higher than the conventional Gilbert cell and offers an error vector magnitude (EVM) improvement of −23 dB at the receiver. This work provides RF designers a comprehensive understanding of system and circuit level on pre silicon base.

Keywords: Low noise amplifier · Radio frequency · Error vector magnitude

1 Introduction

The millimeter wave (mmWave) IEEE 802.11ad standard operating at 60 GHz offers very high throughput of multi Giga bit data [1]. The standard specifies 4 channels each with a bandwidth of 1.08 GHz and uses higher order (even up to 1024) of modulation. Although, mmWave based 5G cellular design would be quite different but developers and designers might use the skills and evaluation/measured data from this 802.11ad standard to understand the functionality of new generation networks [2]. The circuit and radio designer would consider some of the parameters and fine tune the circuits to operate perfectly in cellular system. With multi Giga bit data, the standard is likely to penetrate the indoor environment, hot-spot, airport like location; making it ubiquitous. However, the communication range is very limited to 10 m or so. Additionally, radio frequency (RF) components such as low noise amplifier (LNA), mixer in receiver and power amplifier in the transmitter chain play important role in the overall performance of the system.

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Design of RF components in this mmWave frequency with wide bandwidth, high linearity is challenging. RF impairments in each building block of the receiver would greatly affect the overall performance [3]. Furthermore, any block in the RF chain is heavily dependent on the other circuits [4]. Thus, a system level analysis becomes essential in order to satisfy the requirements of error vector magnitude (EVM) for the wireless standard 802.11ad. EVM measures the distance of the received signal points from the ideal location in a signal constellation and is used to quantify the performance of a transmitter or receiver. Additionally, the higher modulation schemes are adversely affected by RF impairments and reduce the acceptable data rate. This work mainly concentrates on design of RF components in the receiver such as LNA and down converter. The suitability of the designs is analyzed at system level for 802.11ad standard. Particular attention is paid to improve the noise figure, linearity and gain flatness of the receiver blocks.

In this work, a complete direct conversion and heterodyne architecture based transceiver is developed for IEEE 802.11ad [5] using our designed LNA and mixer. Common source (CS) cascade topology is used for LNA. Modified Gilbert cell topology is used for down converter. Various improvements, such as; gain, linearity and isolation are obtained by fine tuning the design. These values are improved from any existing design available in the literature. Furthermore, analysis of each module is carried out for the suitability of IEEE 802.11ad standard. The system level heterodyne receiver including the designed LNA and RF down converter offers an EVM of −32.24 dB for 802.11ad 16QAM baseband signal. A detailed RF budget analysis is carried out to validate the performance of the designed components of LNA and the mixer. The overall NF is 5.377 dB for a heterodyne receiver. IIP3 and SNR of the whole system is −9.688 dBm and 28.26 dB respectively.

The contents of the rest of the paper are as follows. Design of RF components such as LNA and down converter and its nonlinearity issues are described in Sect. 2. System level of heterodyne receiver for 802.11ad wireless standard and specification of each block are presented in Sect. 3. Simulation results and impact of nonlinearity of down converter on EVM are explained in Sect. 4 while, Sect. 5 concludes the paper.

2 Design of Receiver Components

2.1 Design of Low Noise Amplifier

LNA is an important component in any RF receiver and used for amplifying the signal level without increasing the noise floor. One of the key specifications of an LNA is its noise figure. The noise factor is the ratio of actual output noise to that which would remain if the device itself did not introduce noise. The noise figure is the noise factor expressed in decibels (dB) [6]. A common source cascode topology is used for implementing LNA. Though, the topology is common, modification is incorporated to fine tune and obtain enhanced performance. The schematic of 60 GHz LNA is shown

in Fig. 1. The design is completed using 65 nm UMC low leakage, low threshold voltage, CMOS RF transistors (N_12_LLLVTRF). Important design equations of LNA are [7, 8]:

$$Z_{in} = j\omega\left(L_{dg} + L_{TL}\right) + \frac{1}{j\omega C_{gs}} + \frac{g_m L_{TL}}{C_{gs}} \tag{1}$$

$$LL_1 = \frac{1}{\omega^2(CC + C_{ds})} \tag{2}$$

where, Z_{in} is the input impedance. L_{TL} is the inductance corresponds to the transmission line, at the input (tlinp in Fig. 1), which is used to tune out Im$\{Z_{in}\}$ along with degenerative inductor L_{dg}. C_{gs} and C_{ds} are the parasitic capacitances at the gate and drain. CC is the coupling capacitor between stages. Load inductance LL_1 resonates with CC and C_{ds} at the operating frequency ω.

The dimension of the transistors M_0, M_1 are $22 \times 1\,\mu m \times 60\,nm$. The second stage transistors are sized a bit larger in order to provide higher gain. Size of M_2 and M_3 is $26 \times 1\,\mu m \times 60\,nm$. A high transconductance g_m is obtained by maintaining high aspect ratio. Two middle inductors L_{m1} of 87pH and L_{m2} of 73pH are connected in the midway of the cascode structure. Together with parasitic capacitances of the transistors, it increases the unity current gain frequency, f_T to 260 GHz. Figure 2 shows the improvement in f_T with the presence of L_m. The inductors LL_1 of 160pH and LL_2 of 190pH are designed to resonate at fundamental frequency together with c_{ds} of M_1 and M_3 as in Eq. (2) [9]. L_i of 139pH is used for blocking the RF signal from going to the bias circuit. A 97pH of L_{dg} is connected as a degenerating inductor at the source of M_0.

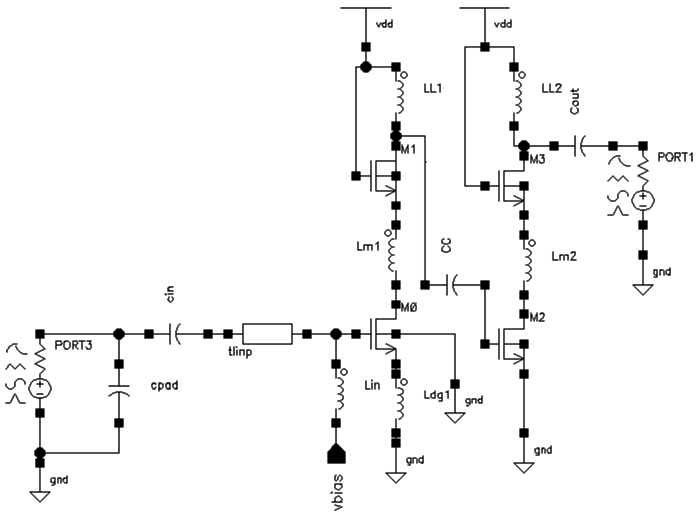


Fig. 1. Schematic of LNA

L_{dg} plays an important role in gain and the stability. A padding capacitance of 25fF, input and output capacitance of 55fF and 38fF respectively are selected as part of the matching network. A coupling capacitor between the stages is chosen to be 210fF to resonate at the operating frequency as in Eq. (2). The presented circuit is designed for a V_{DD} of 1.2 V.

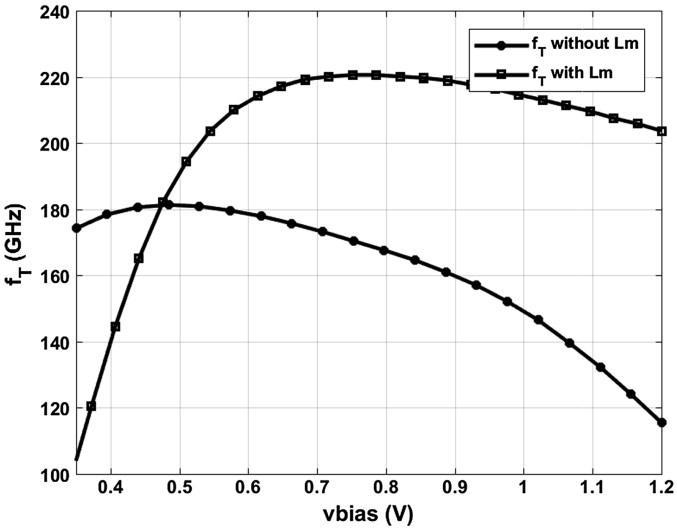


Fig. 2. Improvement on f_T with the presence of L_m.

2.2 Design of RF Down Converter

RF down converters or the mixer performs frequency translation of baseband modulated signals by multiplying it with a local oscillator (LO) signal. Commonly used Gilbert cell is chosen for the frequency down conversion as it has good LO isolation and is the best choice for heterodyne architectures [4]. The basic Gilbert cell mixer is shown in Fig. 3. In this design, we have modified the circuit to enhance the performance.

With the abrupt switching of LO signal, the circuit of down converter produces spurs of RF signal. If the LO signal is not having an abrupt switching, then the down converter will suffer a lower gain and higher noise. Thus LO waveform is chosen to be square wave to ensure abrupt switching and having maximum conversion gain (CG) [4]. The frequency converting action of mixer is characterized by conversion gain or the loss. The voltage conversion gain is the ratio of root mean square (RMS) voltage of the intermediate frequency (IF) output to RF input signal.

The LO transistors are to be switched perfectly for the multiplication function of modulated baseband input signal and LO signal. To get a fast slew rate, we made the swing of LO to be large. LO bias is avoided here for ensuring complete switching off of the balanced pair. Thus, the first step in the design was to device a switching transistor which gives an abrupt switching characteristics.

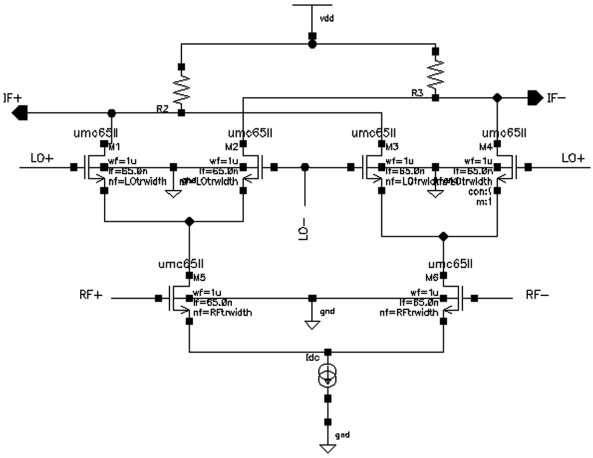


Fig. 3. Basic Gilbert cell down converter

The design uses 65 nm UMC low leakage low threshold voltage, CMOS RF transistors (N_12_LLLVTRF). Each transistor is chosen to have a length of 65 nm and width per finger of 1 µm. The analysis of switching characteristics is done for the carrier frequency of 58.32 GHz as LO frequency, the central frequency of channel 1 in IEEE802.11ad and assured a low rise time. The width of LO transistors (M_1, M_2, M_3, M_4) in Fig. 3 is chosen to be 13 µm with an LO peak to peak of 1 V.

The next step in the design of a down converter is to determine the appropriate size of the RF transistors to trade off noise figure and maximum frequency of oscillation (f_{max}). Maximum frequency of oscillation is commonly used as a figure of merit of the transistors and is defined as the frequency at which the extrapolated power gain falls to unity. The value of f_{max} depends on sizing, bias conditions, as well as transistor resistive loss and layout parasitic [9]. Figure 4 shows the tradeoff of f_{max} and NF.

The RF transistor width is varied from 0.5 µm to 50 µm. Figure 4 shows minimum noise figure and maximum unity gain frequency which can be achieved for a finger width of 17 µm to 30 µm. A supply voltage of 1.2 V and a bias voltage of 0.5 V is chosen [10]. After fixing the bias voltage and number of fingers for minimum NF and maximum f_{max}, the g_m of the RF transistors are made high to get a high conversion gain. The requirement has to be satisfied for a low V_{ds}. Since the power supply is only 1.2 V, there is no enough head room for the V_{ds} of the RF transistors to vary. The transistors are made in saturation region in order to obtain high g_m and low C_{gd} values. Thus as a conclusion, we need to choose a large width for providing high g_m, which will intern help to saturate the transistors at low V_{ds}. For low noise also, large width is preferred. Thus the width of the RF transistors is fixed at 28 µm.

Modified double balanced Gilbert cell is used to achieve high linearity and better return loss. The schematic diagram of the modified Gilbert cell is shown in Fig. 5. A pair of PMOS transistor M_7 and M_8 are used as active load and in order to achieve sufficient bandwidth and gain with the limited voltage head room available. These load transistors are biased to strong inversion region with a width of 29 µm.

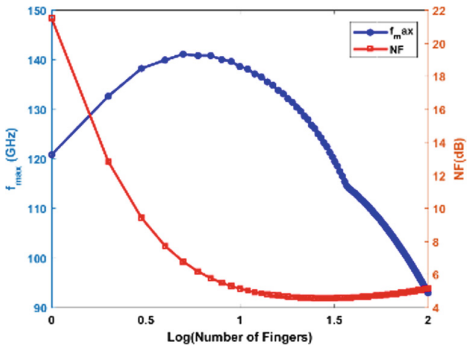


Fig. 4. f_{max} and NF variation with respect to Number of fingers of the RF transistor

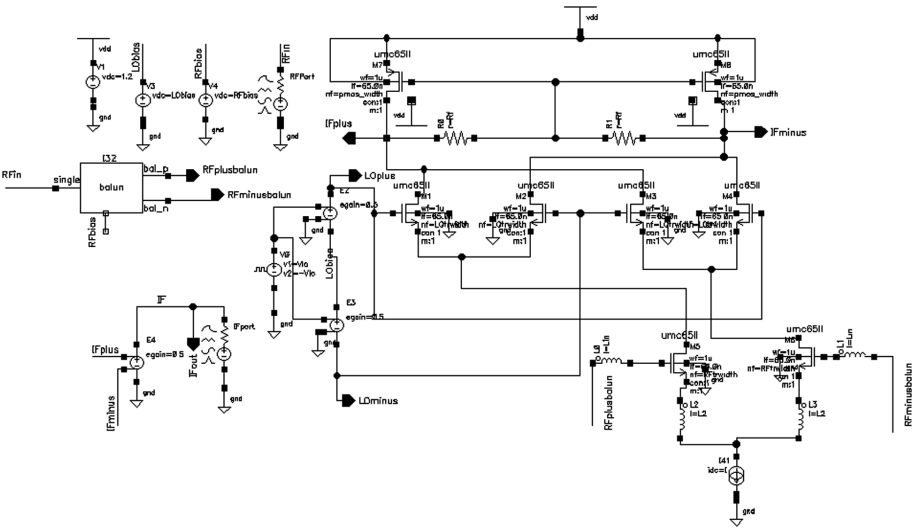


Fig. 5. Modified Gilbert cell

Feedback resistances, R_f is used at the load for high output impedance. This will prevent any decease of CG at low LO power. Degenerative inductors L_2, L_3 and L_0, L_1 at the RF input are used for matching the differential input 50 Ω. The design equation of the matching circuit is given as:

$$Z_{in} = j\omega L_2 + \frac{1}{j\omega C_{gs}} + \frac{g_m L_2}{C_{gs}} + j\omega L_0 \tag{3}$$

where, the variables have usual meaning. Equation 3 is derived with the assumption that C_{gd} is negligible and assume that node between source resistors is at virtual ground. For a perfect match and resonance, equate $\frac{g_m L_2}{C_{gs}}$ *to* $50\,\Omega$ and $\omega^2 = \frac{1}{(L_2 + L_0)C_{gs}}$,

along with a transconductance, $g_m = 20.73\,\text{m}$ and $C_{gs} = 28.57\text{fF}$, L_2 and L_0 are calculated to be $2.0796 * 10^{-10}\,H$ and $1.891 * 10^{-11}\,H$ respectively.

2.3 Nonlinearity Issue of Down Converter

In this paper, the linearity issue in down converter is studied in detail. These RF impairments can be compensated only by the proper designing of RF components. For predicting the effect of RF impairments on receiver performance, a detailed analytical study is required. EVM, a measure of how far the constellation points are from the ideal locations can be evaluated using Eq. (4). The actual constellation points will deviate from its ideal locations by various imperfections in the implementation of transmitter and receiver.

$$EVM = \sqrt{\frac{E\left|v_o - v_{ref}\right|^2}{E\left|v_{ref}\right|^2}} \tag{4}$$

where v_o is the output of down converter and v_{ref} is the reference signal without any imperfections. Here the EVM variation due to the no idealities of the down converter is considered. Any non-linearity in the output of the down converter signal can be expressed as its baseband equivalent signal.

$$v_0 = a_1(v_I + jv_Q) + a_3\left(v_I^3 + jv_Q^3\right) \tag{5}$$

where a_1 and a_3 represent the linear and third order nonlinearity of the I/Q signal gains. IIP3 of a circuit and these gains are related to:

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} \tag{6}$$

The reference signal will be compressed due to the nonlinearity present in the circuit.

$$v_{ref} = C(v_I + jv_Q) \tag{7}$$

where C is the compression factor and is defined as [11, 12]:

$$C = \sqrt{a_1^2 + 2a_1a_3k + a_3^2k^2} \tag{8}$$

and

$$k = \frac{v_1^3 + jv_Q^3}{v_I + jv_Q} \tag{9}$$

Substituting (7), (8) and (9) in to (4),

EVM due to IIP3 can be estimated as

$$\mathrm{EVM}_{\mathrm{IIP3}} = \frac{1}{C}\sqrt{(a_1 - C)^2 + 2(a_1 - C)a_3 k + a_3^2 k^2} \tag{10}$$

when there is no nonlinearity present, $a_3 = 0$ and $C = a_1$; and $\mathrm{EVM}_{\mathrm{IIP3}} = 0$ as expected.

Each impairment affects the overall EVM. The net EVM in a receiver is the contributions due to these circuit no idealities.

$$EVM^2_{overallR} = EVM^2_{\Delta IQ} + EVM^2_{LO} + EVM^2_{IIP3} \tag{11}$$

EVM due to the components in transmitter are not considered here. For example the EVM due to power amplifier's AM-AM conversion and AM-PM conversion are not included in the analysis. EVM degradation due to LO leakage is also discarded as it affects for direct conversion receivers only.

3 System Level Development of IEEE 802.11ad Receiver

A system level simulation of heterodyne receiver is carried out to suit the IEEE802.11ad standard. The frequency allocation of the four channels in 802.11ad and its central frequencies are as shown in Fig. 6. The channel extends from 57.24 GHz to 65.88 GHz and having four channels. Each channel is 1.08 GHz wide and having central frequencies as in Fig. 6. The analysis of RF components and the receiver are carrier out to ensure satisfactory performance in these four channels.

The performance metric of the receiver are error vector magnitude (EVM), signal to noise ratio (SNR), linearity, and the noise figure.

The main challenge in the design of RF components is to reduce EVM by reducing the RF impairments. A stand-alone LNA or down converter design is no longer meaningful as its performance heavily depends on the other circuits in the RF chain.

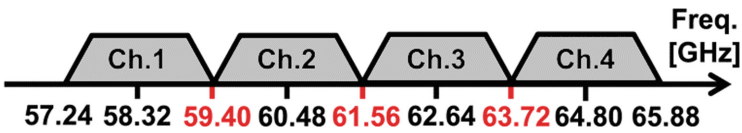


Fig. 6. Channels defined in IEEE 802.11ad standard

Figure 7 shows the architecture of the receiver and its analysis setup for the measurement of EVM in cadence virtuoso environment. The models and the measurement components are chosen from the rfLib.

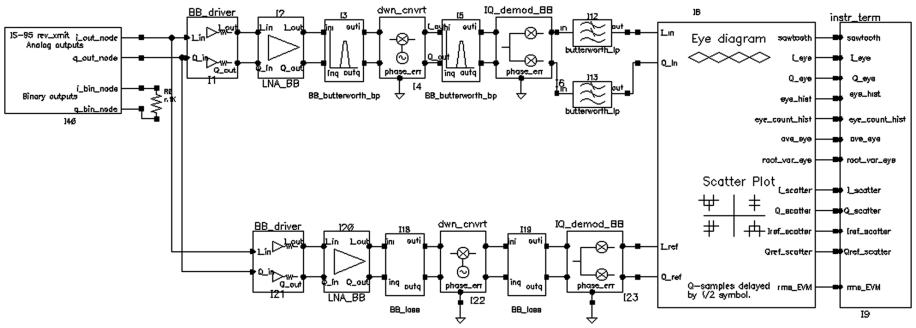


Fig. 7. Architecture of the receiver for IEEE 802.11 ad/ay and a system level performance analysis simulation set up for EVM.

System level receiver is analyzed with designed components and components from references. The obtained receiver EVM with the designed LNA along with mixers in the references are tabulated in Table 1. Table 2 lists the EVM of the receiver with designed down converter and some LNAs from literature. These values are tabulated for channel 1 of IEEE 802.11ad with an LO frequency of 58.32 GHz.

Table 1. Estimated EVM for the receiver with designed LNA along with mixers in references.

Designed LNA specifications	Down converter 1 specifications [5]	Down converter 2 specifications [13]	Down converter 3 specifications [14]
Gain = 20 dB	CG = 1 dB	CG = 0 dB	CG = 2 dB
NF = 1.7 dB	NF = 17 dB	NF = 16 dB	NF = 3 dB
IIP3 = −7.78 dBm	IIP3 = −7.5 dBm	IIP3 = 9.5 dBm	IIP3 = −8 dBm
EVM	−20.4087 dB	−27.5540 dB	−21.9024 dB

Table 2. Estimated EVM for the receiver with designed down converter along with mixers in references.

Designed down converter specifications	LNA 1 specifications [15]	LNA 2 specifications [16]
CG = 1.5 dB	Gain = 14.6 dB	Gain = 18.7 dB
NF = 7 dB	NF = 5.5 dB	NF = 5.2 dB
IIP3 = 8.78 dBm	IIP3 = −6.8 dBm	IIP3 = −6.5 dBm
EVM	−34.1053 dB	−31.9145 dB

The EVM is found to be −32.24 dB using the designed LNA and down converter along with other RF components. Specifications of the RF components other than LNA and down converter are listed in Table 3.

Table 3. Characteristics of other components in the RF chain.

BPF	IF filter	IQ demodulator	LPF
Filter order = 3	Filter order = 3	NF = 2	Filter order = 3
Insertion loss = 3 dB	Insertion loss = 1 dB	I mixer gain = 0 dB	Insertion loss = 0 dB
Central frequency = 57.24 GHz	Central frequency = 1.08 GHz	Q mixer gain = 0 dB	Corner frequency = 1.08 GHz
Relative bandwidth = 37 m	Relative bandwidth = 49 m		

4 Results and Discussions

4.1 Performance of LNA and Down Converter

The designed LNA has a uniform gain of 20 dB around the required band of interest as shown in Fig. 8(a). Input and output return losses S_{11} and S_{22} are both less than −10 dBm in 57–66 GHz band. Wide band matching is achieved using transmission lines. NF is

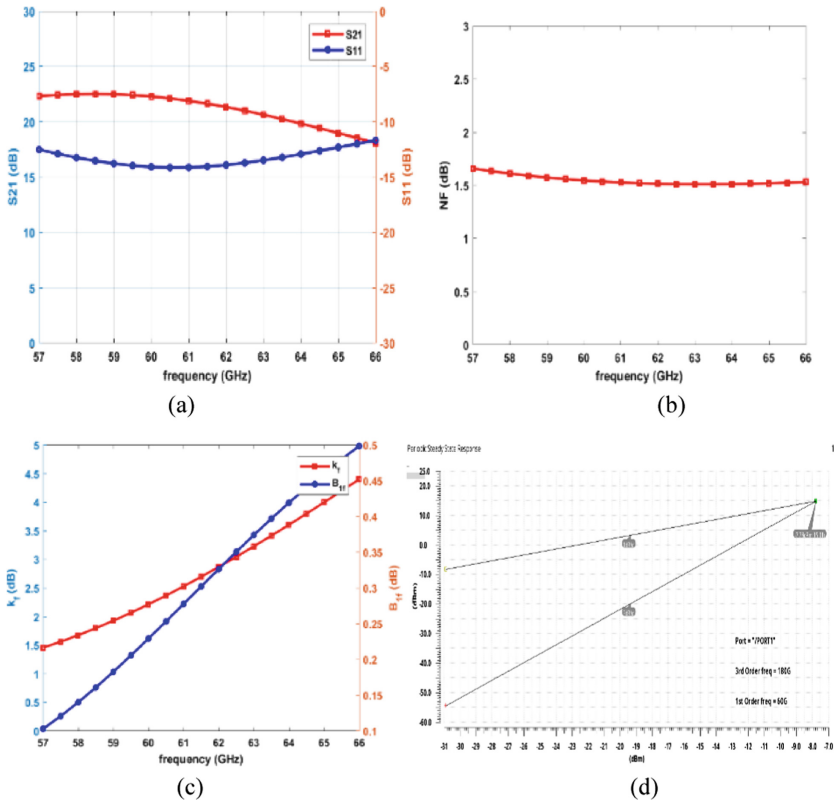


Fig. 8. (a) S_{21}, S_{11}, (b) NF, (c) K_f, B_{1f} and (d) IIP3 of LNA

approximately 1.7 dB as plotted in Fig. 8(b). Figure 8(c) shows that the stability factor (Rollet factor) k_f which is greater than 1 and the alternate stability factor B_{1f} is less than unity for the entire band of interest. Thus, the designed LNA has a very good stable characteristic as it satisfies the stability criteria [8, 17]. IIP3 of LNA is plotted in Fig. 8(d) and is found to be at −7.78 dBm.

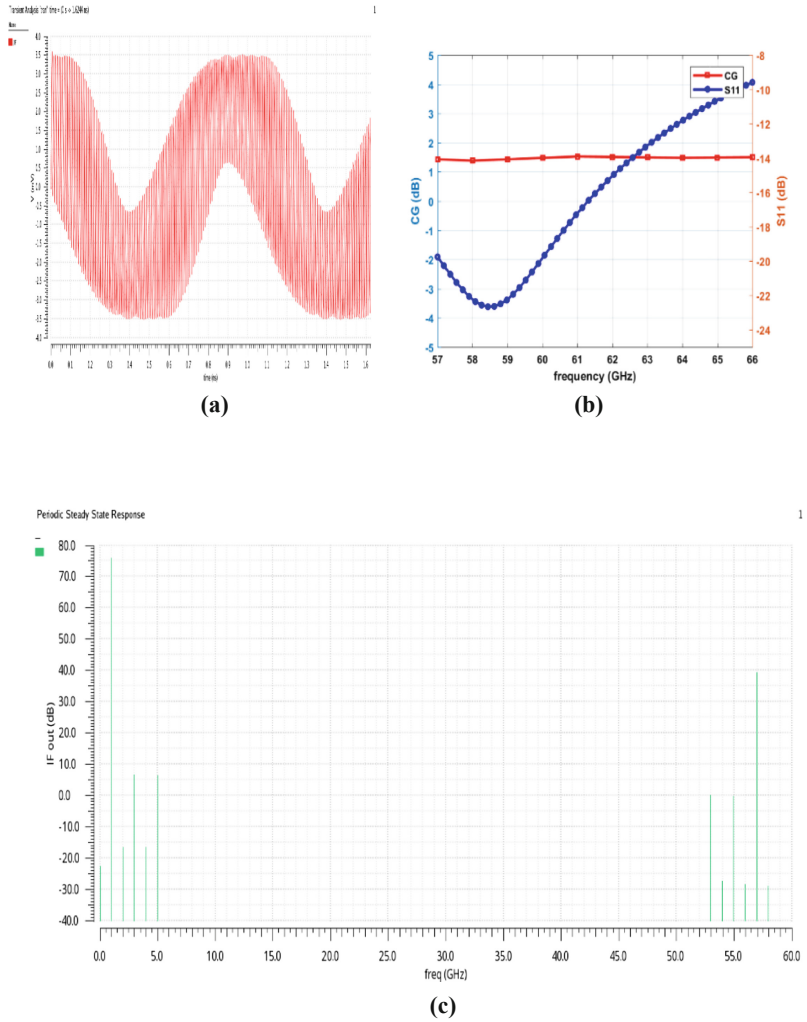
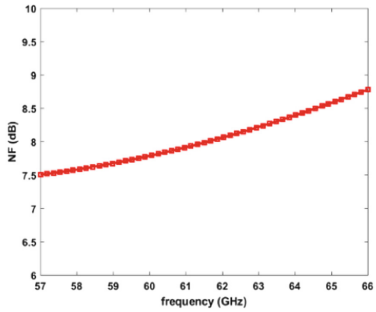
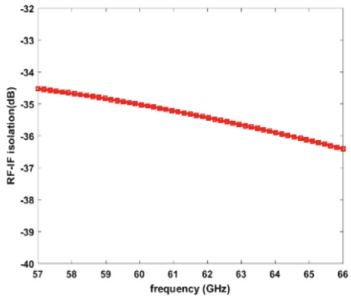


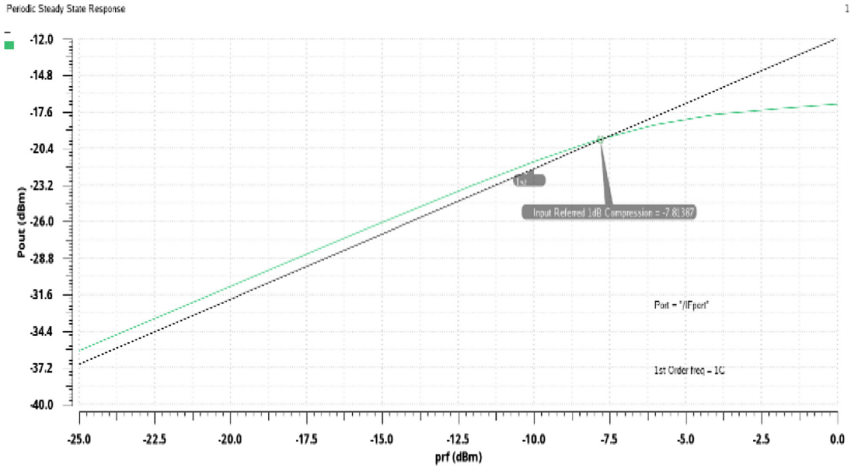
Fig. 9. (a) Mixer output and its spectrum, (b) CG vs RF frequencies and RL, (c) Spectrum of IF output signal, (d) NF for the down converter, (e) RF-IF isolation and (f) P_{1dB} of mixer



(d)



(e)



(f)

Fig. 9. (*continued*)

Down converter output is plotted in Fig. 9a. Since there is matching networks at the RF side, the RF return loss is < −10 dB for the entire band of interest. This is plotted in Fig. 9(b). CG of 1.5 dB is also shown in Fig. 9(b) for the frequency range of 57 GHz to 66 GHz. The spectral purity can be seen in Fig. 9(c). The NF is around 7 dB for the band of interest and is illustrated in Fig. 9(d). Figure 9(e) shows the RF to IF isolation and is around −35 dB. Linearity of down converter, 1 dB compression point, P_{1dB} is found to be at −7.8 and is shown in Fig. 9(f). The simulation results in Fig. 10 shows a significant linearity improvement of IIP3 while maintaining good CG and wide IF bandwidth. The IIP3 of the modified double balanced down converter is found to be at 8.78 dBm and is 10.08 dB more in compared to the conventional Gilbert cell topology having an IIP3 of −2.3 dBm.

Tables 1 and 2 in Sect. 3 also show the comparison of previously reported LNA and RF down converters in various technologies and topologies with the designed LNA and down converter.

4.2 Impact of Nonlinearity of Down Converter on Receiver Performance

The IIP3 of the down converter has been improved from −2.3 dBm to 8.78 dBm by modifying the commonly used Gilbert cell configuration. The EVM was found to be −9.213 dB, for an IIP3 of −2.3 dBm. By improving the linearity of the down converter to an IIP3 of 8.78 dBm, EVM has been reduced to −32.24 dB.

Figure 11 shows the simulated and analytical EVM improvement with respect to different IIP3 values. The deviation in graph is due to the contributions of other components such as EVM due to I/Q imbalance, $EVM_{\Delta Q}$, phase noise of local oscillator, EVM_{LO} as in Eq. (11). Those contributions can be considered as an additive term to the present EVM variation.

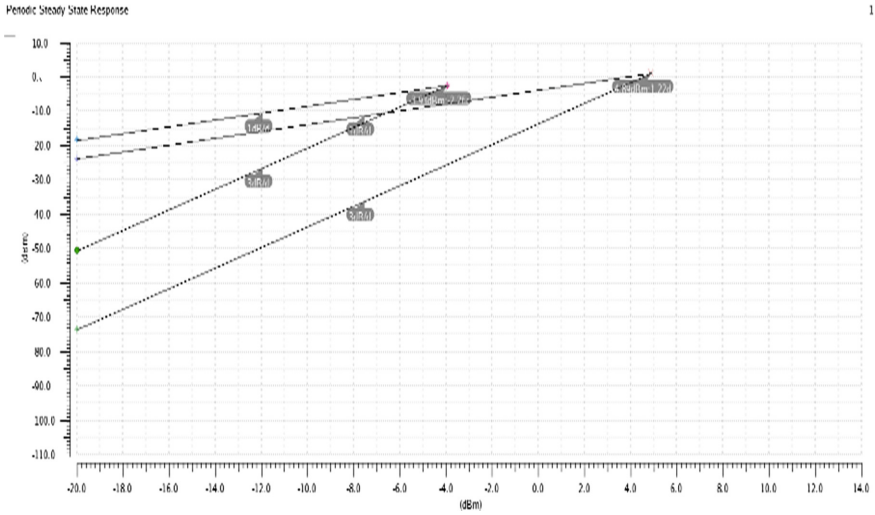


Fig. 10. IIP3 improvement in modified down converter

The constellation of 16QAM signal for EVM of −9.213 dB is shown in Fig. 12(a) and the constellation corresponding to an EVM of −32.24 dB is given in Fig. 12(b).

Table 4 shows the comparison table of receiver in terms of EVM for IEEE 802.11ad channel 1 for 16QAM with the results in [5]. In [5] a complete transceiver is implemented and the measured EVM was −24.6 dB, −23.9 dB, −24.4 dB and −26.3 dB for channel 1, 2, 3 and 4 respectively for 64QAM. For 16QAM, the EVM for the entire transceiver was measured to be −24.6 dB, −24.1 dB, −24.6 dB, −27.0 dB and −17.2 dB for channel 1, 2, 3, 4 and channel 1 to 4 bonding. A 7 dB improvement is observed in comparison with [5].

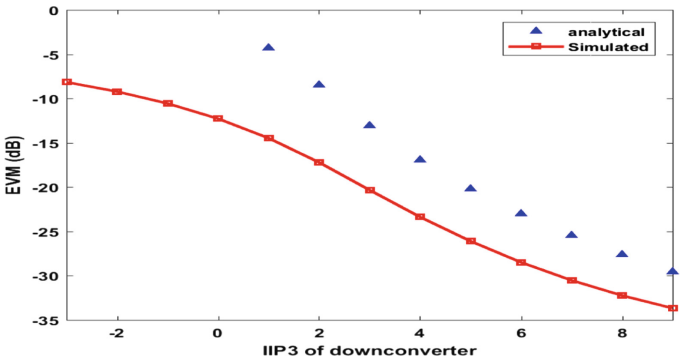
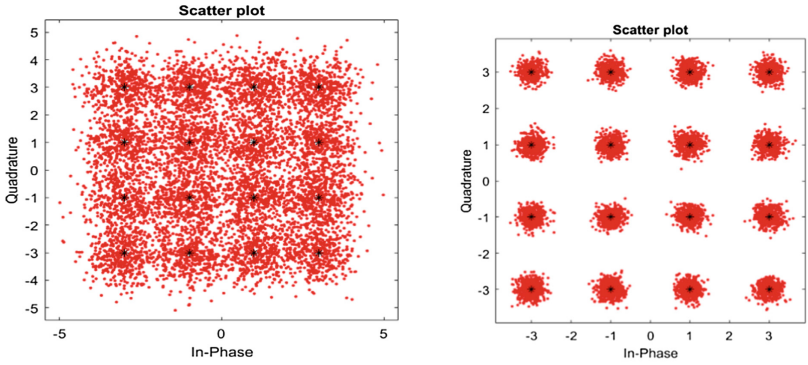


Fig. 11. Improvement in EVM for different values of IIP3 of down converter.

Table 4. Comparison table of the receiver in terms of EVM

	EVM
[5]	−24.6 dB
This work	−32.24 dB

[a][5] is the implementation result of complete transceiver.



(a) (b)

Fig. 12. Constellation of 16QAM for EVM of (a) −9.213 dB and (b) −32.24 dB.

RF budget is calculated for the cascaded receiver in Fig. 7 and is displayed in Fig. 13. The IIP3, NF, Gain of the entire receiver is −10.68 dBm, 5.597 dB and 14.83 dB respectively. SNR of the entire receiver is 28.04 dB. This is reasonably good for a 16QAM modulation to get a bit error rate of 10^{-15} [18].

```
      InputFrequency: 58.32 GHz
 AvailableInputPower:   -50 dBm
     SignalBandwidth:  1.08 GHz
          AutoUpdate: true

Analysis Results
     OutputFrequency: (GHz) [58.32   58.32   58.32    1.08    1.08]
         OutputPower: (dBm) [  -30  -30.66  -33.66  -32.16  -35.17]
      TransducerGain: (dB)  [   20   19.34   16.34   17.84   14.83]
                  NF: (dB)  [  1.7     1.7   5.484   5.597   5.597]
                OIP3: (dBm) [12.22   11.56   8.565   7.161    4.15]
                IIP3: (dBm) [-7.78   -7.78 | -7.78  -10.68  -10.68]
                 SNR: (dB)  [31.94   31.94   28.16   28.04   28.04]
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Fig. 13. RF budget of the receiver

5 Conclusion

An EVM of −32.24 dB is observed for 16QAM in channel 1 of IEEE802.11ad standard. SNR of the entire receiver is 28.04 dB. This is reasonably good performance for a 16QAM modulation to get a bit error rate of 10^{-15}. These performances are supported by flat gain characteristics of LNA and down converter. Designed LNA and down converter has a linearity of −7.78 dBm and 8.8 dBm of IIP3. A return loss lesser than −10 dB ensures the stability criteria. NF of 1.7 dB for LNA and 7 dB for the down converter is also observed. These are improved and optimum performance parameters (based on exhaustive simulation and analysis) for the standard with the modified LNA and mixer. However, with fabricated chip, the performance needs to be evaluated.

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References

1. Kumar, C.S., Priyadharsini, A.R.A., Babuthirumangaialwar, E.: A multi giga bit speed wireless communication standard – IEEE 802.11ad. Int. J. Innov. Res. Sci. Eng. Technol. **3** (3), 1598–1601 (2014)
2. Radio Electronics. https://www.radio-electronics.com/info/wireless/wi-fi/ieee-802-11ad-microwave.php. Accessed 6 July 2018
3. Nitsche, T., Cordeiro, C., Flores, A.B., Knightly, E.W., Perahia, E., Widmer, J.C.: IEEE 802.11ad: directional 60 GHz communication for multi-Gbps Wi-Fi. IEEE Commun. Mag. **52**, 132–141 (2014)
4. Razavi, R.: RF Microelectronics, 2nd edn. Prentice Hall Communications Engineering and Emerging Technologies Series from Ted Rappaport (2013)
5. Wu, R., Minami, R., Tsukui, Y., Kawai, S., Seo, Y., Sato, S.: 64QAM 60 GHz CMOS transceivers for IEEE 802.11 ad/ay. IEEE J. Solid State Circuits **52**(11), 2871–2889 (2017)

6. Chen, H.K., Lin, Y.S., Lu, S.S.: Analysis and design of a 1.6–28-GHz compact wideband LNA in 90-nm CMOS using a π-match input network. IEEE Trans. Microw. Theory Tech. **58**(8), 2092–2104 (2010)
7. Prameela, B., Daniel, A.E.: Design of low noise amplifier for IEEE standard 802.11b using cascode and modified cascode techniques. Procedia Technol. **25**, 443–449 (2016)
8. Pournamy, S., kumar, N.: Design of 60 GHz broadband LNA for 5G cellular using 65 nm CMOS technology. In: 7th International Conference on Communication Systems and Network Topologies (CSNT), Nagpur, pp. 320–324 (2017)
9. Pozar, D.: Microwave engineering, 3rd edn. Wiley, Hoboken (2012)
10. Singh, S., Vasudevamurthy, R., Kumar, N.: Design of wideband 5G millimeter wave mixer in CMOS 65 nm. Accepted in 7th International Conference on Advances in Computing, Communications and Informatics (ICACCI 2018), pp 19–22, September 2018
11. Nassery, A., Ozev, S., Slamani, M.: Analytical modeling for EVM in OFDM transmitters including the effects of IIP3, I/Q imbalance, noise, AM/AM and AM/PM distortion. In: 2013 18th IEEE European Test Symposium (ETS), Avignon, pp. 1–6 (2013)
12. Gupta, A.K., Buckwalter, J.F.: Linearity considerations for low-EVM, millimeter-wave direct-conversion modulators. IEEE Trans. Microw. Theory Tech. **60**(10), 3272–3285 (2012)
13. Zhu, F., Hong, W., Chen, J.-X., Jiang, X., Wu, K.: A broad band low power millimeter wave CMOS down conversion mixer with improved linearity. IEEE Trans. Circuits Syst. **61**(3), 138–142 (2014)
14. Zhang, F., Skafidas, E., Shieh, W.: A 60 GHz double balanced Gilbert cell down conversion mixer on 130 nm CMOS. In: 2007 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Honolulu, HI, USA. IEEE (2007)
15. Lee, C.-H., Choi, W., Kim, J.-H., Kwon, Y.-W.: A 77 GHz 3-stage low noise amplifier with cascode structure utilizing positive feedback network using 0.13 μm CMOS process. JSTS: J. Semicond. Technol. Sci. **8**(4), 289–294 (2008)
16. Yao, T., Gordon, M., et al.: Algorithmic design of CMOS LNAs and PAs for 60-GHz radio. IEEE J. Solid State Circuits **42**(5), 1044–1057 (2007)
17. Kraemer, M., Dragomirescu, D., Plana, R.: A low-power high-gain LNA for the 60 GHz band in a 65 nm CMOS technology. In: 2009 Asia Pacific Microwave Conference, Singapore, pp. 1156–1159 (2009)
18. Homepage Dsp log, http://www.dsplog.com/2007/12/09/symbol-error-rate-for-16-qam/, last accessed 2018/7/6