A 70-W Asymmetrical Doherty Power Amplifier for 5G Base Stations

Ahmed M. Abdulkhaleq[1,2(✉)], Yasir Al-Yasir[2], Naser Ojaroudi Parchin[2], Jack Brunning[1], Neil McEwan[1], Ashwain Rayit[1], Raed A. Abd-Alhameed[2], James Noras[2], and Nabeel Abduljabbar[2]

[1] SARAS Technology Limited, Leeds LS12 4NQ, UK
a.abd@sarastech.co.uk
[2] Faculty of Engineering and Informatics, Bradford University, Bradford BD7 1DP, UK
r.a.a.abd@bradford.ac.uk

Abstract. Much attention has been paid to making 5G developments more energy efficient, especially in view of the need for using high data rates with more complex modulation schemes within a limited bandwidth. The concept of the Doherty power amplifier for improving amplifier efficiency is explained in addition to a case study of a 70 W asymmetrical Doherty power Amplifier using two GaN HEMTs transistors with peak power ratings of 45 W and 25 W. The rationale for this choice of power ratio is discussed. The designed circuit works in the 3.4 GHz frequency band with 200 MHz bandwidth. Rogers RO4350B substrate with dielectric constant εr = 4.66 and thickness 0.035 mm is used. The performance analysis of the Doherty power amplifier is simulated using AWR MWO software. The simulated results showed that 54–64% drain efficiency has been achieved at 8 dB back-off within the specified bandwidth with an average gain of 10.7 dB.

Keywords: Asymmetrical Doherty Power amplifier · Drain efficiency GaN HEMTs · Wireless communications · LTE-Advanced

1 Introduction

The requirement for increasing the amount of transmitted data within a limited bandwidth using mobile communications systems is growing rapidly and this is expected to continue, especially with the developments of the LTE-Advanced system, where the user is being attracted by the video streaming and multimedia data in addition to the Internet of Things technology revolution [1–3]. Hence the 5G mobile generation will include several technologies that can help to achieve the promised goals of the 5G. Some of these are the use of massive MIMO, carrier aggregation, beam forming and more complex modulation schemes which produce a high peak to average power ratio (PAPR). The high PAPR requires the power amplifier to be backed off from the most efficient point into a region where the efficiency drops sharply. As a result, a large amount of supply power will be dissipated as a heat [1]. In particular, a high efficiency performance produces a low linearity of the power amplifier and vice versa. The power

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amplifier should be designed to produce high efficiency at a large Output power Back-off (OBO). There are several techniques which are used for efficiency enhancements, and these include Envelope Tracking (ET), Envelope Elimination and Restoration (EER), LInear amplification using nonlinear Component (LINC), Chireix outphasing, and the Doherty Power amplifier. However, the simplest technique is the Doherty amplifier, where neither additional controlling circuits nor signal processing blocks are required [3].

The present paper has four sections, starting with the Doherty concept, then a Doherty design example appropriate to 5G, followed by the simulation results and finally the work's conclusions.

2 Doherty Concept

The Doherty combiner was introduced by its inventor W.H. Doherty in 1936 [4] in relation to high power tube amplifiers for broadcasting station. Nearly linear output power can be achieved using two or more power amplifiers by combining their outputs with λ/4 transmission lines. The Classical Doherty power amplifier consists of two separate amplifiers known as the carrier amplifier and the peaking amplifier (Fig. 1). The carrier amplifier is designed to operate as a class AB amplifier whereas the peaking amplifier is designed to operate as class C amplifier. The input signal is split between the two amplifiers, where the carrier amplifier should be saturated at the back-off input power; at the same power level, the peaking amplifier starts feeding current to the output till it becomes saturated at the peak region, where the two power amplifiers give their maximum designed output power [5–7].

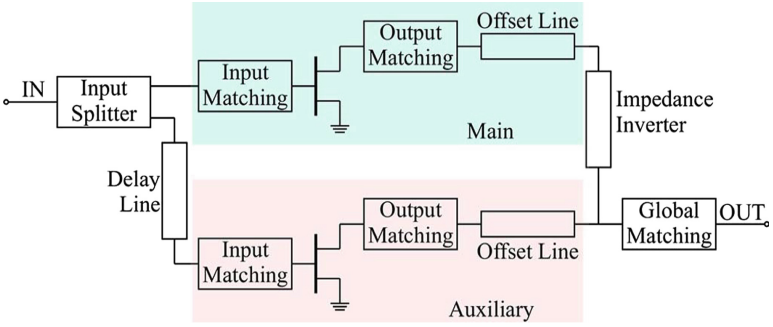


Fig. 1. Doherty Power amplifier structure [2]

The idea of the Doherty depends on the so-called active load-pull technique [1]. Where the operation of the Doherty power amplifier can be divided into three main regions [5–9]:

The low power region, where the input signal level is not sufficient to turn the peaking amplifier on so that the peaking amplifier can (ideally) be represented as an open circuit. On the other hand, the main amplifier is amplifying the input signal as an

ordinary power amplifier, however the load is seen by the main amplifier through the λ/4 transmission line (Impedance Inverter), which makes the main amplifier saturate because it sees a high load impedance at this phase, as shown in Fig. 2(a). The impedance seen by the main amplifier depends on the following equation,

$$Z_1 = \frac{Z_T^2}{R_L} \tag{1}$$

where:

Z_1: the impedance seen by the main amplifier
Z_T: the impedance of the λ/4 transmission line
R_L: the load impedance

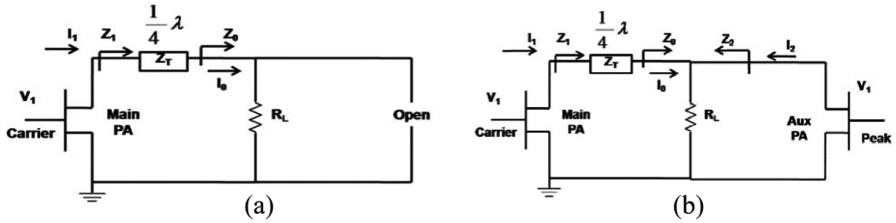


Fig. 2. Doherty operation region [2] (a) Low power region, (b) Medium and high-power region

The second region (medium power region) where the peaking amplifier starts injecting the current into the load and acts as a current source. As the current in the peaking amplifier increases, the load impedance seen by the impedance inverter will be increased, at the same time, the impedance seen by the main amplifier will be decreased. As a result, the main amplifier output voltage remains roughly constant and the total current is increasing which increases the total output power as shown the following equations:

$$Z_2 = R_L\left(1 + \frac{I_\circ}{I_2}\right) \tag{2}$$

$$Z_1 = \frac{Z_T^2}{R_L\left(1 + \frac{I_2}{I_\circ}\right)} \tag{3}$$

where:

Z_2: the impedance seen by the Peaking amplifier
$I_\circ$: the current after the λ/4 transmission line
I_2: the peaking Amplifier current

Finally, the high-power region, where both amplifiers work at their maximum output current, where the impedance seen by each amplifier is controlled by Eqs. (2) and (3).

The current and voltage behaviour of both the main and the peaking amplifiers is shown in Fig. 3. It can be observed that the peaking amplifier starts injecting the current near the OBO point, whereas the voltage of the main amplifier remains roughly constant after the OBO point but its current increases.

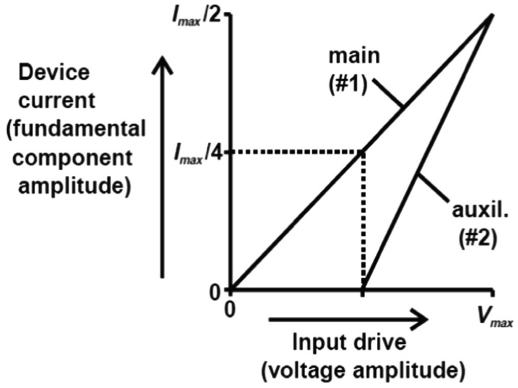


Fig. 3. Main and peaking current amplitude [1]

3 Doherty Design

As mentioned above, the main amplifier should be designed as class AB, whereas the peaking amplifier should be biased as a class C power amplifier. The first issue in designing any power amplifier is to take into account the stability of the transistor to make sure it does not oscillate. Then the input and output matching networks have to be designed for the optimum load and source impedances that achieve the best transistor performance.

Since the peaking amplifier is not behaving as a current source when it is off, but it is still subject to the output capacitance of the intrinsic device and the parasitic elements of its package, the offset line should be inserted at the output of the peaking amplifier to ensure that a high impedance will be seen when the peaking transistor is off below the back-off region, as this is one of the main conditions to satisfy the Doherty concept. After adding the offset line in the output of the peaking amplifier, the phase difference should be compensated by inserting an offset line at the output of the main amplifier.

An important issue in designing the Doherty power is the transistor choosing, which is govern by the following parameters

1. The average power
2. The PAPR

The summation of both parameters determines the maximum output power of the Doherty power Amplifier i.e. the sum of the main and peaking output power, whereas the PAPR represents the same amount of the back-off power that can define the ratio between the peaking amplifier to the main amplifier according to the following equation

$$B = -20\log(1+\delta) \tag{4}$$

where

δ: is the ratio of the peaking power amplifier to the main power amplifier.

For this paper, the maximum output power was 70 W with an –8 dB back off, so that the ratio δ should be at least 1.5. So that, GaN HEMTs transistors with peak power ratings of 45 W and 25 W are satisfying the design requirements.

Another issue in the Doherty power amplifier design is the line offset, where the output impedance of the peaking amplifier should be high, so that a line offset will be added to the output impedance of the peaking amplifier, its electrical length for this deign case is 29.2°.

4 Simulation Results

A 70 W Doherty power amplifier analysis and performance are simulated using AWR MWO software. Rogers RO4350B material was used as a substrate. The full circuit schematic is shown in Fig. 4 whereas the layout of input and output matching circuits for both main and peaking amplifiers are shown in Fig. 5.

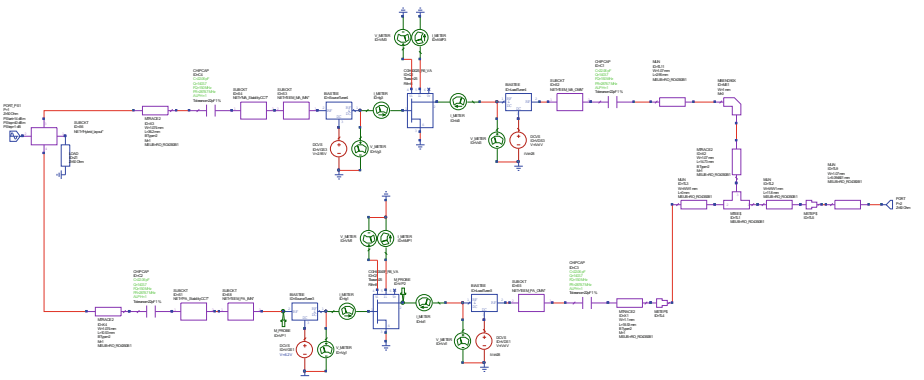


Fig. 4. Full circuit schematic

The performance of the main and peaking amplifiers separately in terms of output power, gain, drain efficiency and Power added efficiency (PAE) are shown in Fig. 6 and Fig. 7 respectively. As illustrated in Fig. 6, about 80% drain efficiency is obtained from the main amplifier with an average gain of 10 dB. Nevertheless, the performance of the peaking amplifier shown in Fig. 7, represents a class C power amplifier where it can be noticed that the peaking amplifier starts injecting the power after the input back-off point.

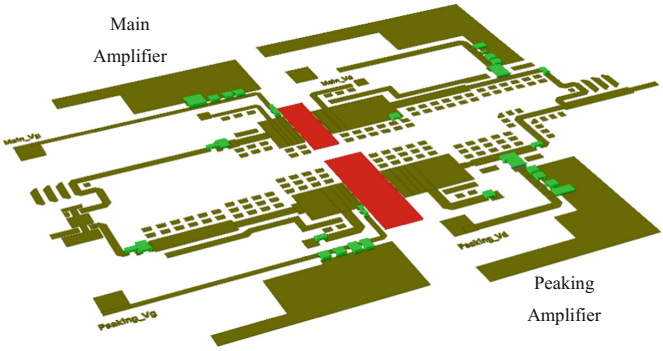


Fig. 5. Input and output matching circuit for Doherty Power amplifier

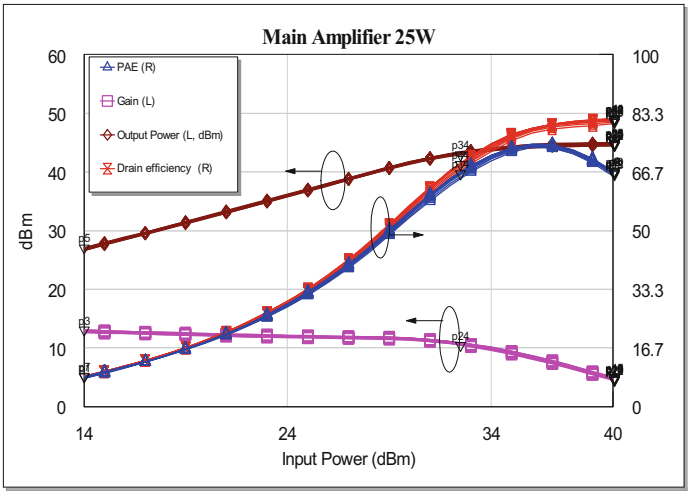


Fig. 6. Main amplifier performance

Furthermore, it can be notice from Fig. 8, the line offset is needed to produce a high impedance seen from the combiner toward the output of the peaking amplifier when the transistor is off in order to satisfy one of the Doherty conditions. It can be noticed that a high impedance can be gotten by adding a line offset.

In addition, it can be noticed from Fig. 9 that the designed Doherty power amplifier has about 63% drain efficiency at 8 dB OBO for 3.4 GHz; however, the efficiency level for other frequencies is less due to the effect of the off-set lines. At the same time, the gain obtained is 10.8 dB. In addition, the total output power of the designed Doherty power amplifier is 48 dBm where both amplifiers participate with their full power.

The achieved simulation results are compared with other works over the same frequency band, as shown on Table 1.

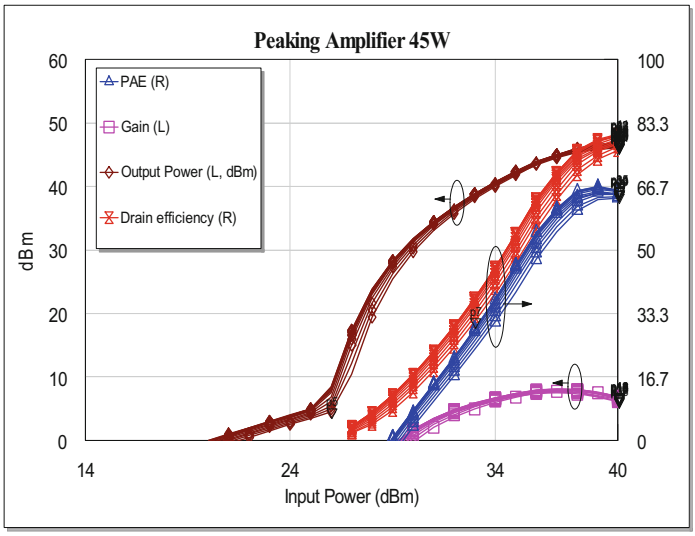
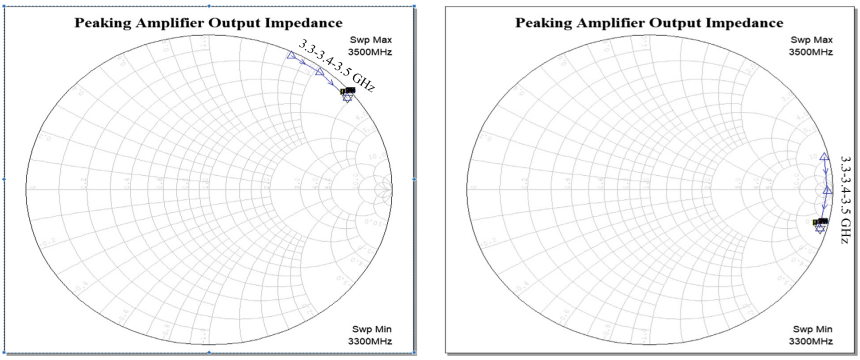


Fig. 7. Peaking amplifier performance



(a) (b)

Fig. 8. Peaking output impedance seen from the far end when the transistor is off (a) without line offset (b) with line offset

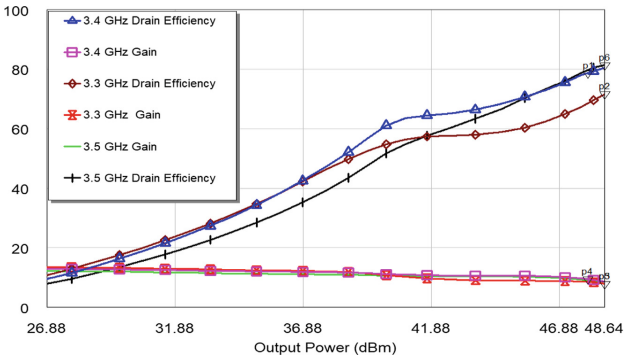


Fig. 9. Doherty power amplifier efficiency

Table 1. Previous work achievements

	Frequency (GHz)	P_{sat} (dBm)	P_{av} (dBm)	OBO (dB)	DE @OBO	Gain dB
[6]	3.3–3.6	43	37	6	38–56[a]	10
[7]	3.4–3.6	43	35	8	63	12.5
[8]	3.35–3.5	49.3	41	8	50.2–55.1	14.75
[9]	3.4–3.6	44.5	36.5	8	40–42[a, b]	25
This work	3.3–3.5	48	40	8	54–64	10

[a]Practical measurements
[b]Power added efficiency @ OBO

5 Conclusions

The Doherty power amplifier provides the simplest way of combining two amplifiers to provide a good efficiency performance around the back off region. The performance of A 70 W Asymmetrical Doherty power amplifier was simulated using AWR MWO; the overall Doherty power amplifier showed, as per design, an 8.3 dB OBO, with 40 dBm average power. The Drain efficiency at the back off point was 63%, whereas the average gain was 10.7 dB.

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