Fast Statistical Modelling of Temperature Variation on 28 nm FDSOI Technology

Abdelgader M. Abdalla[1(✉)], Isiaka A. Alimi[1], Manuel González[2], Issa Elfergani[1], and Jonathan Rodriguez[1]

[1] Instituto de Telecomunicações, Department of Electronics, Telecommunications and Informatics (DETI), Universidade de Aveiro, 3810-193 Aveiro, Portugal
{a.m.abdalla,i.t.e.elfergani,jonathan}@av.it.pt, iaalimi@ua.pt
[2] Evotel Informatica SL, Madrid, Spain
m.gonzalez@evotel-info.com

Abstract. It is well known that the 28 nm fully depleted Silicon-On Insulator (FDSOI) node has a temperature effect due to the inherent pyroelectric and piezoelectric properties. In this paper, we introduce a spatial interpolation Lookup table (LUT) model considering temperature dependence of nanometer CMOS transistors. The novel methodology is used to build the bias current and capacitance LUTs for MOS transistor circuits under extensive variety of temperature values, evaluated under transient analysis. This innovative LUTs model significantly reduce the simulation runtime with sufficient accuracy using adaptive multivariate precomputed Barycentric relational interpolation for the appraisal temperature effects of 28 nm FDSOI node.

A transient analysis benchmark is employed in order to verify and validate the proposed models according to the well-known simulation models (i.e. the 28 nm FDSOI model and traditional spatial Lagrange model). The proposed model can significantly reduce the size of lookup table, thereby reducing the computational cost. Furthermore, the model outperform the 28 nm FDSOI compact physical model and the traditional spatial Lagrange model due to the reduced simulation runtime by up to eight orders of magnitude considering the temperature effect in 28 nm FDSOI innovation. Moreover, the proposed novel LUT based approaches are able to attain high precision with much reduced computational cost.

Keywords: Statistical modelling · Temperature variation
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1 Introduction

The 28 nm FDSOI node is a promising nano-CMOS technology offering several benefits such as reduction in power, space scaling, cost effective platform and performance enhancement. It also enables a lower VDD and acts as an electrostatic

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enhancer to reduce the short channel effects; and provisions for better energy management, thanks to an ultra-thin buried oxide (BOX) and body biasing characteristics over the counterpart conventional Bulk technology [1]. The body biasing feature is vastly efficient for adjusting the transistor channel, tolerating the optimization of dynamic and static power consumption [1]. In spite of its predominant attributes, operation of the 28 nm FDSOI node fluctuates when the temperature changes in relation to the climatic conditions; the materials utilized have inborn pyroelectric and piezoelectric properties that help in influencing its attributes and consequently the circuit performance [2]. The temperature performance of the logic gates and input-output (IO) cells planned depend on FDSOI transistors [3]. A switch in the working temperature causes the mobility to vary and prompts changes in the on-current Ion, threshold voltage VT, and velocity saturation in each device [4]. In this aspect, ordinary compact and physical transistor models, such as Fe-FETs, BSIM, and PSP, comprise a substantial number of parameters and complicated equations in order to characterize the physical mechanisms, beyond the typical characterization for a short-channel device [4–6]. These sort of models have a high level of complexity and offer high precision mirroring the fundamental device physics. All things considered, they together, back-off the evaluation runtime. On the other hand, the empirical behavioral models of the circuit simulation depend on the LUT models. The LUT models comprise of the device input-output qualities and utilize some reasonable numerical interpolation, as well as numerical strategies to get working point values from the LUTs within the simulation process [7–10]. The LUT technique is simple to implement [11,12]. Nevertheless, it requires a high density of data points, which lead to an expansion in the computational cost in the request procedure. In recent times, a novel LUT approach in view of a spatial Lagrange polynomial has been introduced in [13]. The foremost benefit of this approach, is that, numerical model can be obtained from the measured information set. Besides, it has a characteristic ability at the highest order of polynomial for any given arrangement of information. The use of this method (i.e. spatial Lagrange polynomial) to build behavioral transistor model with just a single expression gives an insight into the device behavior over the whole area of biasing and in all areas of operation as well as considering process, voltage and temperature (PVT) variation. Therefore, by exploiting this method, just one equation is required for characterizing the transistor considering all gates-biasing voltages within a high range of temperature, and for both the triode and saturation operation regions of the I-V characteristics [3,13]. However, the principle downside of this technique, is that all work will be tunneled towards recalculating every single degree of the polynomial. This is not compatible with the wide deployment of multi-core architectures. Therefore, researchers have shown an increased interest in sequential optimizations algorithm if and only if it is effective in the perspective of parallel performance. In this paper, we adopt Barycentric rational interpolation because of ease of implementation using adaptive multivariate precomputed method that results in faster simulation and stability [15,16]. Moreover, this method (i.e. Barycentric rational interpolation) has recently attracted an enormous community of both end-users and

developers from diverse disciplines. For example, standard optimization software like DAKOTA employs Barycentric rational interpolation for efficient global optimization of stochastic black-box systems [17,18]. This proposed model (i.e. Barycentric rational interpolation) is employed to build LUTs for both current-voltage (I-V) curve and capacitance-voltage (C-V) profile of a transistor as well as transconductance gm over an extensive variety of temperatures. Simulation results are given considering 28 nm FDSOI node. We compare this against legacy methodologies such as conventional Lagrange interpolation, and the compact physical transistor level model portrayed by 28 nm FDSOI in Cadence, exploiting the 5th degree of the polynomial for measuring both the I-V and C-V curve. Such an approach significantly simplifies the transistor model. Additionally, it decreases the computational cost by five orders of magnitude in the transient analysis without loss of fidelity.

This paper is organized as follows: in Sect. 2, mathematical formulas of the DC model for classical Lagrange, and Barycentric rational interpolation are briefly reviewed. Also, novel LUT approaches and their implementation details are discussed; Sect. 3 introduces small signal modeling for the extraction gate -source C_{gs}, drain-source C_{ds}, and gate-drain C_{gd} as well as transconductance g_m; Sect. 4 describes the system analysis; and in section V, model validation and simulation runtime are discussed and verified in transient analysis by comparing simulation results obtained in terms of output current, voltage, and simulation runtime with the measured model and conventional Lagrange.

2 DC Modeling

The dc model needs an appropriate expression to accurately describe and predict the measured current-voltage (I-V) characteristics over a wide temperature range. First we introduce the traditional recursive Lagrange, and Barycentric rational interpolation formulas. Subsequently, the proposed dynamic programming procedure which we developed by both Barycentric rational interpolation is given. The Lagrange interpolating polynomial. Initially, the Lagrange interpolating polynomial, indicated by $P(x)$, is one of a kind polynomial of degree m for which $P(x_i) = f(x_i)$ for $i = 0, 1, \ldots, m$. This can be expressed as [13]:

$$P(x) = \sum_i L_i \cdot f(x_i) \tag{1}$$

where $(x_0, x_1, x_2, x_3, \ldots\ldots)$ and $(x_0, x_1, \ldots, x_m)$ are the nodal points, and the Lagrange coefficient, $L_i(x)$ is given by [9]:

$$L_i = \prod_{j=0, i\neq j}^{m} \frac{(x - x_j)}{(x_i - x_j)} \tag{2}$$

The coefficients have various properties that are suitable to be considered [13]. Lagrange coefficient formed for the $m+1$ points $(x_0, y_0), (x_1, y_1) \ldots (x_m, y_m)$ is a polynomial of degree m which vanishes at $x = x_0 \ldots\ldots x = x_{i-1}, x = x_{i+1}$ however,

when $x = x_i$, the value of the multiplier will be 1 (one). The type of the Lagrange coefficient in (refeq2) demonstrates that it depends just on the given x's and is completely free of the y's [14]. We employed the mentioned Lagrange definition of the univariate to elicit the tensor product of the I_{ds} drain current as a function of the gate to source voltage V_{gs} and temperature T, regarding Lagrange polynomial are expressed as follows:

$$I_{ds}(V_{ds}, V_{gs}, T) = \sum_{i=0}^{n} \sum_{j=0}^{m} f(V_{ds}, V_{gs}, T = T_i) \cdot L_{ij}(T_i, V_{gs_i}) \tag{3}$$

where V_{ds}, are the drain to source voltage. For L_{ij} the Lagrange multipliers can be stated as follows:

$$L_{ij}(T, V_{gs}) = L_i(T) L_j(V_{gs}), \;\; 0 \leq i \leq n, \;\; 0 \leq j \leq m \tag{4}$$

$$L_i(T) = \prod_{\tau=-n, \tau \neq i}^{n} \frac{(T - T_\tau)}{(T_i - T_\tau)} \tag{5}$$

$$L_j(V_{gs_j}) = \prod_{\rho=0, \rho \neq j}^{m} \frac{(V_{gs} - V_{gs_\rho})}{(V_{gs_j} - V_{gs_\rho})} \tag{6}$$

so, we have

$$L_{ij}(T_\tau, V_{gs_\rho}) = \begin{cases} 1 & i = \tau, j = \rho \\ 0 & \text{otherwise} \end{cases} \tag{7}$$

3 Barycentric Rational Interpolation

The traditional Lagrange interpolation has specific limitations in terms of computational cost since each interpolation requires $O(n^2)$ additions and multiplications; increasing accuracy requires addition of a new data pair that results in the calculation of whole new LUTs. This makes the scheme to be numerically unstable, especially for higher order systems. These limitation are compensated by Barycentric rational interpolation [16]. Also, evaluation of each interpolation requires $O(n^2)$ additions and multiplications. We adopt Barycentric Lagrange interpolation because it is fast and stable [16]. This is due to the pre-computed techniques of the Barycentric weights that reduce its computational complexity to $O(n)$ compared to $O(n^2)$ operations of the conventional Lagrange [16,18].

The univariate of the Barycentric rational formula (sometimes called second (true) form of the barycentric recipe) $P(x)$ is stated as follows [16]:

$$P(x) = \frac{\sum_{j=1}^{n+1} \frac{w_j}{x - x_j} f_j}{\sum_{j=1}^{n+1} \frac{w_j}{x - x_j}} \;\; , j = 1, \ldots, n+1 \tag{8}$$

where w_j is Barycentric weights. The symmetry in Eq. (8) shows that the interpolant $P(x)$ can be computed fast in $O(n)$ operations [16]. This weight is defined as:

$$w_j = \prod_{j=0, j \neq k} (x_j - x_k)^{-1} \tag{9}$$

In order to build the LUT for the proposed model based on Barycentric rational interpolation, we consider multivariate of a continuous function f, i.e. $I_{ds} = f(I_{ds_{ij}}|_{(V_{gs},V_{ds},T)})$ for $i = 1, ..., n$and $j = 0, ..., k$. The drain current I_{ds} for this method is stated as follows [17]:

$$I_{ds}(I_{ds_{ij}}|_{(V_{gs},V_{ds},T)}) = \frac{\sum_{\tau=1}^{\alpha+1}\sum_{r=1}^{b+1} f(I_{ds_{ij}}|_{(V_{gs},V_{ds},T)})M}{\sum_{\tau=1}^{\alpha+1}\sum_{r=1}^{b+1} M} \tag{10}$$

where $M = \frac{w_{\tau r}(V_{gs_j},V_{ds},T=T_i)}{\phi_{\tau r}(V_{gs_j},V_{ds},T=T_i)}$

$$\phi_{\tau r}(\cdot) = \phi_{\tau}(V_{gs} - V_{gs_j})\phi_r(T - T_r) \tag{11}$$

where $w_{\tau r}(\cdot)$ are tensor product of Barycentric weights and can be expressed as:

$$w_{\tau r}(I_{ds_{ij}}|_{(V_{gs},V_{ds},T)}) = w_{\tau,\alpha}(I_{ds_c}|_{(V_{gs},V_{ds})})w_{r,b}(I_{ds_q}|_{(V_{gs},V_{ds},T)}),\ 0 \le c \le \alpha\,, 0 \le q \le r \tag{12}$$

where $w_{\tau,\alpha}(\cdot)$, $w_{r,b}(\cdot)$ are the subsets of the precomputed Barycentric weights for drain current I_{ds} with respect to the temperature variation, and defined as follows:

$$w_{\tau,\alpha} = \prod_{\tau=1,\tau\neq c}^{\alpha+1} (V_{gs_\tau} - V_{gs_c})^{-1}\,, w_{r,b} = \prod_{r=1,r\neq q}^{b+1} (T_r - T_q)^{-1} \tag{13}$$

4 Small Signal Modeling

The 28 nm FDSOI node small-signal equivalent circuit suitable for low frequency process is depicted Fig. 1. It constitutes the intrinsic and extrinsic components for capacitance gate-source C_{gs} , drain-source C_{ds}, and gate-drain C_{gd}. Also it comprises transconductance g_m, gate, source and drain series resistances R_g, R_s and R_d , respectively [20]. Keeping in mind the end goal to guarantees the charge conservative of 28 nm FDSOI node, the capacitance models are set to be a component of the cross voltage (V_{gs}, V_{ds}) [21]. The previously mentioned capacitances are separated by means of two-port multibias s-parameter estimations at 3 GHz converted into y-parameters as defined [22]:

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = j\omega \begin{bmatrix} C_{gs} + C_{gd} & -C_{gd} \\ C_{dg} - C_{gd} & C_{ds} - C_{gd} \end{bmatrix} \tag{14}$$

The detailed of the aforementioned equations and all extraction conditions are expressed in [23]. The partner capacitance conditions of (3) and (10) are reformulated and expressed as follows:

$$C_{ts}(V_{ds}, V_{gs}, T) = \sum_{i=0}^{n}\sum_{j=0}^{m} f(V_{ds}, V_{gs}, T = T_i) \cdot L_{ij}(T_i, V_{gs_i})\ t = g, d \tag{15}$$

$$C_{ts}(I_{ds_{ij}}|_{(V_{gs},V_{ds},T)}) = \frac{\sum_{\tau=1}^{\alpha+1}\sum_{r=1}^{b+1} f(I_{ds_{ij}}|_{(V_{gs},V_{ds},T)})M}{\sum_{\tau=1}^{\alpha+1}\sum_{r=1}^{b+1} M} \quad t = g, d \tag{16}$$

The adaptive univariate precomputed LUT proposed method (i.e. Barycentric rational algorithm) is employed in order to build the multivariate LUTs models for the capacitances C_{gs} , C_{ds}, and C_{gd} as well as transconductance g_m by means of small signal analysis.

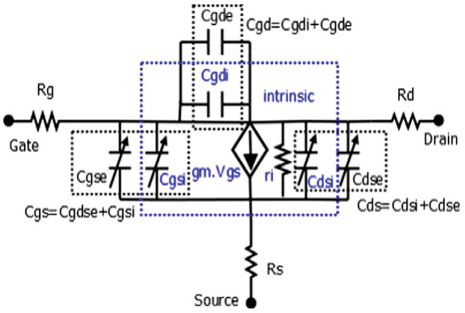

Fig. 1. Comprehensive small-signal equivalent circuit, exploited for the extraction of the extrinsic (represented 'e') and intrinsic (represented 'i') parameters of 28 nm FDSOI node

5 System Analysis

The models have been assessed on 28 nm FDSOI and the same device dimensions as those of in [20] are utilized for simulations. Figure 2 demonstrates the I-V coordinates of the model at the 28 nm FDSOI node with zero body bias and 1.5 V supply voltage, for both PMOS and NMOS devices. At −50 °C, the drain current (I_{on}) is 4.8 mA, though it ascends to 6.2 mA at 120 °C for a gate voltage $V_{gs} = 1.5$ V. This is because of the temperature reliance of the drain current having impact via the threshold voltage and channel mobility as $I_{ds}(T) - \mu(T)[V_{gs} - V_T]$. The $[V_{gs} - V_T]$ term is the set-off drain current that increases with rise in temperature due to the threshold voltage reducing with temperature, as a result of significant errors in the 4th degree of the proposed models as stated in the previous work [14]. This error is reduced with the 5th degree estimate which demonstrates great concurrence with the measured information as appeared in Fig. 2(c–d).

Figure 3 (a–d) shows intrinsic capacitances and transconductance extracted from measurements (black), transitional Lagrange model and the proposed model (i.e. Barycentric rational algorithm). The entire results show excellent match between the proposed approaches and the measured model, as well as the conventional Lagrange model.

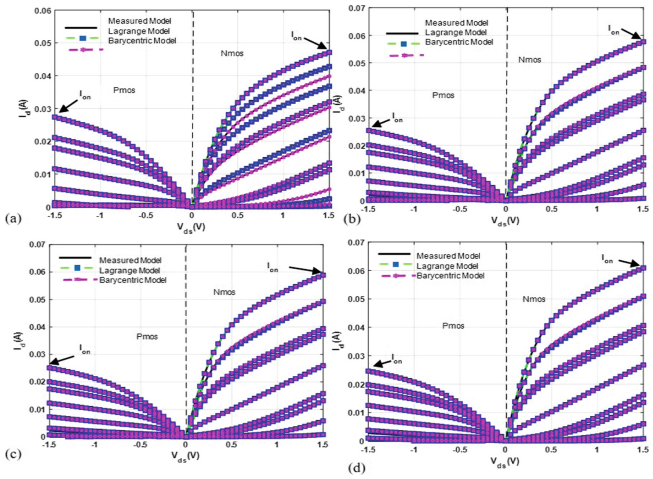

Fig. 2. $I_{ds} - V_{ds}$ characteristics of 28 nm FD SOI: for 5 order (a) −50 °C(b) 60 °C(c) 80°C (d)120 °C

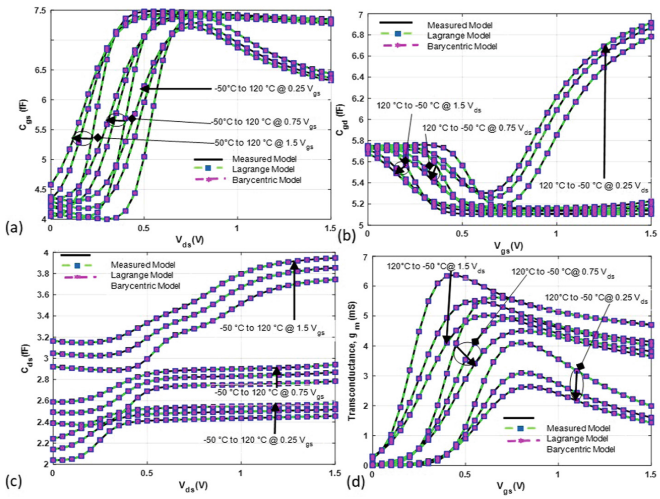

Fig. 3. Intrinsic capacitances and transconductance extracted from measurements (black) , Lagrange model and proposed models matching evaluation for 28 nm FDSOI node: (a) C_{gs} (b) C_{gd}, (c) C_{ds}, (d) g_m

6 Model Validation and Simulation Runtimes

A transient analysis benchmark is used in the inverter circuit in order to verify and validate the proposed models over the BSIM SOI model and traditional spatial Lagrange model as shown in Fig. 4(a) and (b) . The results indicate a great

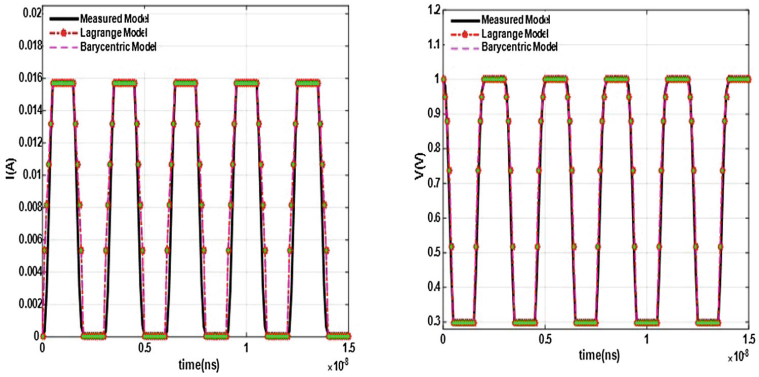

Fig. 4. Precision comparison: verify and validate the proposed models over the 28 nm FD SOI model and traditional.

Table 1. Model simulation runtime compared with 28 nm FDSOI model and the lagrange model in transient simulation

	28 nm FDSOI			Lagrange			Barycentric rational algorithm		
	Step	Time(s)		Step	Time(s)		Step	Time(s)	
		T = −50 °C	T = 120 °C		T = −50 °C	T = 120 °C		T = −50 °C	T = 120 °C
4-bit static Adder	6500	200	245	6505	195	240	6505	20.5	26.7
8 stage NAND	7505	216	260	7506	210	256	7506	22.3	26.1
Inverter	4501	125	165	4507	120	161	4507	12.4	12.4

agreement between the forecasted values of the current and voltage at the output port, which affirms the good precision of the modelling, and the correctness of the model definition, portrayal, and extraction strategy. In addition, with this adequate precision, the two proposed approaches (i.e. Barycentric rational interpolation) can reduce the simulation runtime by up to eight orders of magnitude. This is as a result of the boost in the setup time due to the dynamic programming approach developed by both Barycentric rational algorithms as indicated in Table 1; the Dynamic programming methodology remarkably enhances the simulation proficiency. Simulation runtime assessments are achieved in transient analysis using various benchmark circuits in SPICE. The CPU running time are compared between the proposed models and the 28 nm FDSOI model, as well as the spatial Lagrange interpolation LUT base model. Table I demonstrates that the proposed models have not less than eight orders increase in simulation runtime in contrast to both the spatial Lagrange interpolation LUT and the 28 nm FDSOI model; this is due to the reduction in computational cost, which is as a consequence of the dynamic programming developed by both Barycentric rational algorithms. This progress of computational cost is significantly vital when the whole number of transistors continue expanding in a VLSI circuit [24]. All these results designate that the proposed model enhances model competence significantly without loss of fidelity.

7 Conclusion

The temperature models of the 28 nm FDSOI is discussed and verified with the measured data of both n- and p-channel devices from −50 °C to 120 °C. Using simple adaptive multivariate precomputed developed by Barycentric rational interpolation to extrapolate I-V and C-V, the models achieves reduced simulation runtime with excellent accuracy in circuit analysis. Furthermore, the proposed models can enhance the simulation runtime by up to eight orders of magnitude and beyond without loss of fidelity.

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