**Table 3:** Comparison the normalize leakage power loss in ISCAS-85 benchmark circuits when sleep time is from 0.01µs to 5µs at 100°C.

| Sleep time (µs) | C432 | | | C499 | | | C880 | | |
|---|---|---|---|---|---|---|---|---|---|
| | SSPG | CRPG | DSPG | SSPG | CRPG | DSPG | SSPG | CRPG | DSPG |
| 0.01 | 1.05 | 4.22 | 1 | 1.05 | 5.22 | 1 | 1.05 | 4.21 | 1 |
| 0.1 | 1.2 | 1.21 | 1 | 1.24 | 1.22 | 1 | 1.23 | 1.19 | 1 |
| 1 | 1.53 | 1.2 | 1 | 1.49 | 1.14 | 1 | 1.47 | 1.13 | 1 |
| 5 | 1.65 | 1.38 | 1 | 1.43 | 1.1 | 1 | 1.56 | 1.49 | 1 |

## 4. Conclusion

Among various power gating technique, we have compared 3 power gating schemes in terms of power delay product, energy loss, wake-up time using the 45-nm Predictive Technology Model. The comparison results show that the DSPG is smaller energy loss, lower power delay product, faster wake-up time than the other power gating schemes. Based on these advantages, we suggest the DSPG as a viable candidate suitable to a fine-grain leakage control scheme, where logic blocks go in and out very frequently and shortly between the active and sleep modes.

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