

Dynamic Voltage-Frequency Scaling in Body Area Sensor Networks using COTS Components

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ABSTRACT

Body area sensor networks (BASNs) have implicit stringent power requirements to meet battery life and form factor expectations, especially in long-term medical monitoring applications. The largest power consumer in BASNs is typically the wireless transceiver, so recent research has focused on increasing on-node signal processing to reduce the number of bits for wireless transmission. This shift increases the importance of power efficient signal processing. Given that the processing workloads and throughput requirements can change dynamically in a BASN, dynamic voltage-frequency scaling (DVFS) becomes an attractive option for providing the necessary processing rate with the minimum power. However, commercial off the shelf (COTS) components typically used in BASN nodes are not designed for DVFS. This paper characterizes the DVFS capabilities of a COTS processor commonly used on BASN nodes – the TI MSP430 – and explores the usefulness of these capabilities within the context of BASN applications.

Keywords

COTS, DVFS, Dynamic Voltage Scaling, Dynamic Frequency Scaling, Microcontrollers, BASNs, BSNs, BASNs

1. INTRODUCTION

As is the case in most wireless sensor networks (WSNs), wireless transmission of sensed data is the largest power consumer in most current BASNs. This problem is particularly acute in medical BASN applications, in which sensor data rates are high relative to many WSN applications. However, significant power reduction can be achieved through the development of on-node signal processing and data management, thus dramatically reducing the number of bits to be transmitted. This includes not only traditional compression, but advanced signal processing techniques, such as pattern classification and feature detection algorithms. Low power signal processing therefore becomes increasingly important to BASN power efficiency.

Assume that E_r is a ratio of the average energy to transmit one bit

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(E_{tx}) to the average energy to process one bit (E_{proc}). This ratio is typically large (i.e. $E_r \gg 1$) and is determined by a number of factors, including processor energy per operation, the signal processing algorithm and implementation, the packet organization and coding, the networking protocol, etc. Also assume that the compression ratio (CR) achieved by on-node signal processing is the ratio of the number of raw bits to the number of transmitted bits. The ratio of average processing energy (E_{proc}) to average total energy (E_{total}) is therefore:

$$\frac{E_{proc}}{E_{total}} = \frac{E_{proc}}{\frac{E_{tx}}{CR} + E_{proc}} = \frac{1}{\frac{E_r}{CR} + 1} \quad (1)$$

Figure 1 plots this ratio as a function of CR for different values of E_r . It is clear that the importance of low power signal processing increases with more effective pre-transmission compression techniques, even at high E_r ratios.

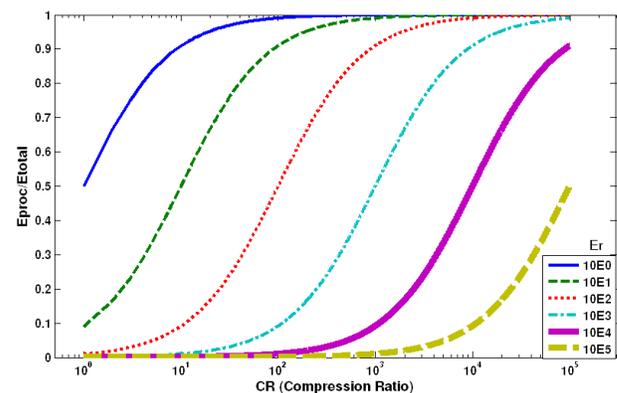


Figure 1: Percentage of total energy contributed by on-node signal processing for different E_r ratios as a function of CR .

1.1 BASN Dynamics

Many data streams in BASN applications, such as physiological and motion phenomena, are highly dynamic, so the signal processing techniques employed over time and the CRs achieved will change. For example, the severity of Parkinsonian tremor fluctuates dramatically over time and across different activities. Figure 2 shows a ten second window of the vector magnitude acceleration from a triaxial accelerometer sensor node on the wrist of a Parkinson's Disease subject. This window reveals an

intentional tremor (a tremor brought on by some intentional movement), and the frequency and amplitude components of the tremor are significantly different than the components pre-tremor [1]. Depending on the specific application and the information that is expected to be relayed to the base station, different processing techniques may be used and CRs achieved once the tremor is detected.

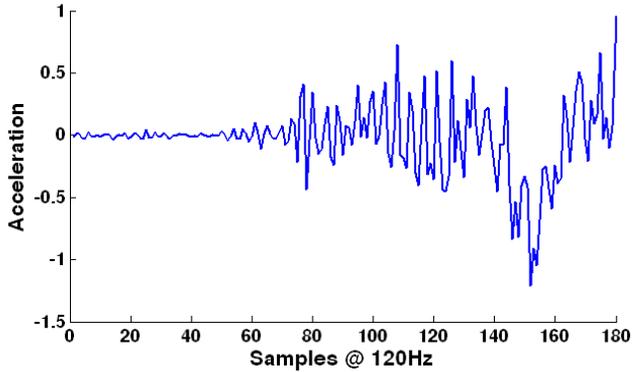


Figure 2: Parkinson tremor from clinical trials.

In addition to the dynamic nature of sensed data, the dynamic operating conditions of a BASN can affect how on-node signal processing is performed. Body absorption and movement create rapidly varying wireless channel conditions with sometimes severe signal attenuation [2]. Unlike many traditional WSNs, the body is a dynamic surface that changes shape and enters different environments throughout the runtime of a BASN. It has been shown that simple variations in posture and sensor placement on the body can amount to over 50 dB differences in signal receive strength across the body with 2.4 GHz technology [3, 4]. Empirical measurements regarding channel loss due to sensor node placement on the body are shown in Figure 3. As the wireless channel capacity fluctuates, so may the on-node processing requirements. Rather than varying transmit power in a transceiver to account for such fluctuations in wireless channels [5], one could alter the on-node signal processing and sacrifice application fidelity to achieve a higher CR.

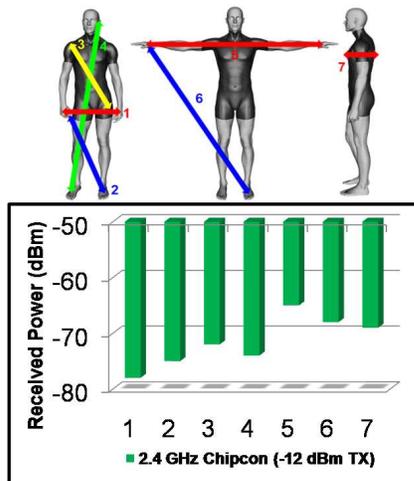


Figure 3: 2.4 GHz received power for different node placements.

1.2 DVFS in BASNs

The dynamic nature of BASNs can be leveraged to achieve power efficient, on-node signal processing through DVFS. However, most COTS components that are used on BASN nodes are not specifically designed for DVFS operation. This paper uses the TI MSP430 as a case study to determine the efficiency of DVFS on a COTS component common to BASN nodes, including the power savings that are achieved at different voltage-frequency pairs and the time and energy overhead of switching between pairs. This study will provide a framework for employing DVFS in BASNs using COTS components, enabling researchers to leverage the dynamic nature of sensed data and operating conditions to further improve the power efficiency of BASNs.

The rest of the paper is organized as follows. In Section 2, we discuss the theory and potential benefits of DVFS, particularly as it relates to BASNs. Section 3 describes a custom platform that was developed for this study. The platform includes a COTS microcontroller commonly used in the BASNs. Section 4 presents and analyses measured DVFS results, which form the basis of a mathematical model that predicts the efficacy of applying DVFS techniques in different BASN application scenarios, including the energy overhead of switching operating levels to analytically determine break-even points. Finally, Section 5 discusses the impacts and conclusions of this study.

2. BACKGROUND

DVFS addresses the issue of application variability by allowing for power savings when timing requirements and/or computational requirements are relaxed. Frequency scaling alone can give a significant benefit, but when paired with voltage scaling, the effect can be enhanced [6]. (Note: voltage scaling cannot be used without frequency scaling because lower source voltages increase gate propagation delays and, therefore, reduce the maximum operating frequency.) In addition, since DVFS minimizes the amount of energy required per processing operation, under the constraint that operations complete “just in time”, it is more effective at saving energy than alternatives that involve the processor running at full speed to complete an operation, then sleeping for the remainder of the available time. This is because the dynamic power consumption of a CMOS circuit is linearly related to the operating frequency and quadratically related to supply voltage:

$$P_p = C \cdot V_{DD}^2 \cdot F \cdot \alpha \quad (2)$$

where P_p is the average power consumption of the processor, C is the total load capacitance being switched, V_{DD} is the supply voltage, F is the operating frequency, and α is an activity factor between zero and one based on the probability of the capacitive load undergoing a 0 to 1 transition during any given clock period. The additional leakage energy from staying in active mode for a longer time does not start to outweigh the dynamic energy savings at current technology nodes until V_{DD} is in the sub-threshold region [7], which is below the voltage range considered in this study.

In the past, typical DVFS operation has been realized using custom chip designs or high end microprocessors that are not appropriate for BASN platforms. While custom chip DVFS is effective in terms of energy efficiency, design and manufacturing

costs are extremely high. These non-recurring engineering (NRE) costs must be amortized across a large volume, and while many BASN applications show great promise, few are currently at the scale to justify custom chip fabrication. COTS devices are attractive system design alternatives due to the low initial investment in components and wide availability. For BASN applications in the research phase, they offer an especially attractive alternative to custom chip designs.

The TI MSP430 family of ultra-low power mixed-signal microcontrollers is used in many BASN applications and platforms [8, 9] offering 16-bit precision with low-power consumption and a large amount of available support. The TI MSP430 and other similar microcontrollers, have on-board clock generation hardware that allows the CPU to programmatically change the operating clock frequency. This is accomplished in the MSP430 through the use of a Digitally Controlled Oscillator (DCO) which may be calibrated using a low frequency (32 kHz) watch crystal as a reference. Once calibration is performed, suitable constants may be stored in on-board flash memory. Frequency agility is then accomplished in a straightforward manner by loading these constants into two clock control registers. The actual change in clock frequency occurs within approximately 10 μ s. Furthermore, this microcontroller operates over a wide range of voltages. The clock oscillator may be varied over a 16 to 1 range and the supply voltage over a 2 to 1 range. Within this envelope, a huge combination of processing rate and power requirements exists, making COTS embedded processors of this type ideal candidates for inclusion in a DVFS scheme for BASNs. This research uses the MSP430 as a case study for implementing DVFS on COTS microcontrollers since it is both widely used in the BASN community and capable of operating at and switching between multiple voltage levels and operating frequencies. With other hardware, the results in this paper may change, so more research may be warranted to investigate the characteristics of other platforms.

3. APPROACH

3.1 MSP430 Scalability

In this research, we explore the MSP430F2131's region of operation in which both the clock and supply voltage may be varied. According to the datasheet, operating frequency can be scaled linearly as a function of voltage for V_{DD} values ranging from 1.8 to 3.3 volts, which correspond to a maximum operating frequency range of 6 MHz and 16 MHz. While the processor can operate well below 6 MHz, it cannot reliably operate below 1.8 volts for V_{DD} , limiting lower frequency operation to dynamic frequency scaling (DFS). Over the range possible for DVFS, the relationship between V_{DD} and F_{DCO} can be expressed as [10]:

$$F_{DCO} (Hz) = (6.67 \cdot V_{DD} - 6.0) \times 10^6 \quad (3)$$

3.2 Hardware Design

For this study, we focus primarily on the power consumption issues related to the microcontroller itself. The efficiency of the voltage regulator circuitry will not be considered in detail, our rationale being that we must first quantify the abilities of the microcontroller to justify any decisions related to a power control scheme. In addition, we will not consider any issues of scheduling

or real-time constraints, although it is clear that such issues exist and are of increasing complexity in application specific environments in which the data processing requirements may vary. This paper seeks to characterize the COTS processor for DVFS capabilities so that BASN developers might apply it to applications and establish scheduling and control techniques.

In an effort to keep external circuitry to a minimum, we employed a common low-dropout adjustable linear voltage regulator in combination with a digital potentiometer to provide an adjustable power supply with fine grained resolution of output voltage. Lastly, in order to give the execution platform a level of electrical energy consumption self-awareness, a "coulomb counter" was included that delivered pulses to the microcontroller at a rate proportional to the supply current.

The LTC4150 from Linear Technology is the coulomb counter used in this study. It finds primary application in battery management circuits and is widely available. It delivers a low-going pulse of $\sim 5\mu$ s width at a rate that is proportional to the voltage developed across two sampling resistors. The transfer function for this portion of the circuit, given by the component datasheet, is [11]:

$$1Pulse = \frac{1}{162.5} Coulombs \quad (4)$$

This pulse is used to generate an interrupt to the microcontroller via the interrupt capabilities of the general purpose I/O pins. On board timing derived from the 32 kHz watch crystal may be used to determine the interval between pulses for current measurement, or the total number of pulses over a specified operating period may be counted and used to calculate total energy consumption.

The TPS76901 from Texas Instruments is an adjustable voltage regulator with a low quiescent current of 12 μ A typical. Note that this is two orders of magnitude lower than the current consumption of the microcontroller in the range of frequency and voltage that we are considering.

The digital potentiometer is an AD5161 from Analog Devices. Communication with the device is through an I²C bus. This bus is a standard for inter-chip communication and is widely used in industry for interconnecting such peripherals as flash memories, analog to digital converters, parallel port expansion chips, and digital potentiometers. An interesting point of design is the level shift circuitry employed to interface 5 volt I²C levels on the AD5161 to the variable V_{DD} levels from the microcontroller, shown in Figure 4 [12]. M1 and M2 operate as bi-directional common gate switching devices. Note the I²C bus is passive pull-up/active pull-down, which eliminates any possibility of destructive bus contention. When either side of the MOSFET is driven low, it forward biases the gate relative to the channel, and turns the device on. The circuit prototype is shown in Figure 5.

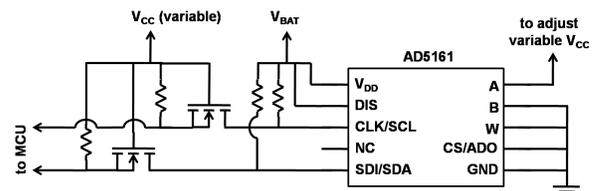


Figure 4: I²C level shifting hardware schematic.



Figure 5: COTS-DVFS hardware prototype.

3.3 Firmware

As with any embedded design, considerations in firmware must deal with the physical realities of the associated hardware. This is especially true for communications on the I²C bus in this design. Consider the oscilloscope traces (Figure 6) for a sample communication used to adjust the digital potentiometer.

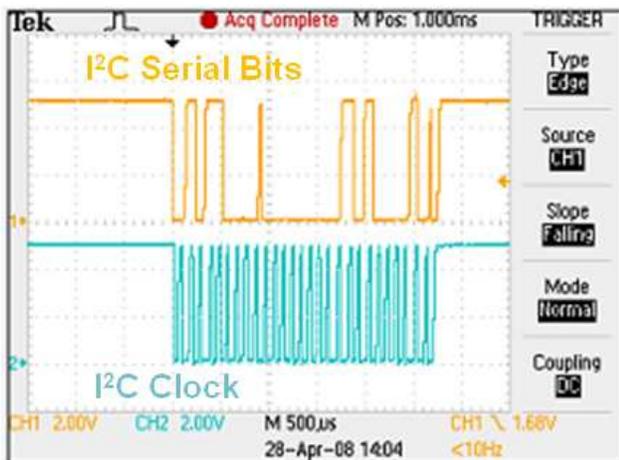


Figure 6: Full I²C communication sequence for adjusting the digital potentiometer (bottom = CLK, top = SDI/SDA).

The data bits are on the top and the clock signal is on the bottom. The entire communication takes slightly over 2.5 ms and must be kept below a maximum bit rate determined by RC constants of the external circuitry. As the time taken to write to the I²C device has a direct impact on the energy overhead for switching voltage levels, it is also desirable to minimize communication time while guaranteeing proper operation of the attached hardware. Consider timing from several individual bits in the data stream above, shown in Figure 7.

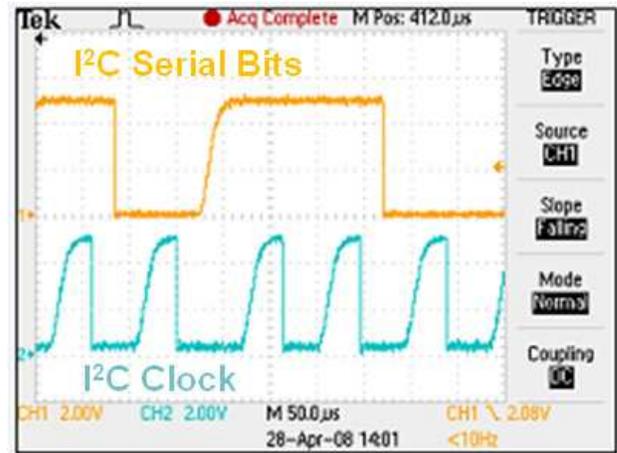


Figure 7: Individual bit timing for I²C communication with the digital potentiometer (bottom = CLK, top = SDI/SDA).

Due to the passive pull-up of the bus, rise times are dramatically longer than fall times. Our operating firmware dynamically determines the appropriate timing for each bit, speeding up the clock when two or more successive ones are sent, and delaying the clock on a 0 to 1 transition of the data. In addition, since the whole I²C transmission is carried out in software, appropriate delays for each possible state are stored in a lookup table, and the delays are adjusted for the current processor clock frequency. The various pause values are adjusted as multiples of a base rate determined by the lookup process.

4. EVALUATION

4.1 Experimental Setup

Two experiments were conducted in order to show both steady-state and transient behavior of the COTS-DVFS system. In the steady state analysis, MSP430 power consumption was measured as V_{DD} and F_{DCO} are varied both separately and together, showing the power consumption for the “voltage-frequency pairs” that would be used in a COTS-DVFS implementation as well as other possible operation scenarios with processor frequencies below the maximum. From these tests, MSP430 energy per operation can also be derived, which establishes the number of cycles needed for the system to “break-even” in energy consumption given any voltage-frequency switch. In other words, switching between any two voltages for less than the break-even cycles would result in energy loss.

The transient analysis attempts to illustrate the overheads associated with switching back and forth between any two voltages. Firmware was designed to switch between two voltages at a time so that oscilloscope readings could be recorded and the transient waveforms could be seen for both increasing and decreasing V_{DD} . The observation of oscilloscope readings as well as knowledge about the designed hardware can be used to construct a simplifying equation (Equation 9) that describes the energy overhead consumed in the system. Another set of firmware was designed to validate the simplified energy overhead equation, and from this, break-even cycles were calculated.

4.2 Steady State Analysis

The minimum voltage for F_{DCO} s between 6MHz and 16MHz is specified by solving Equation 3 for V_{DD} . Using these voltage-frequency pairs, the power consumption of the MSP430 is shown in Figure 8 (the round data points) as V_{DD} and F_{DCO} are swept.

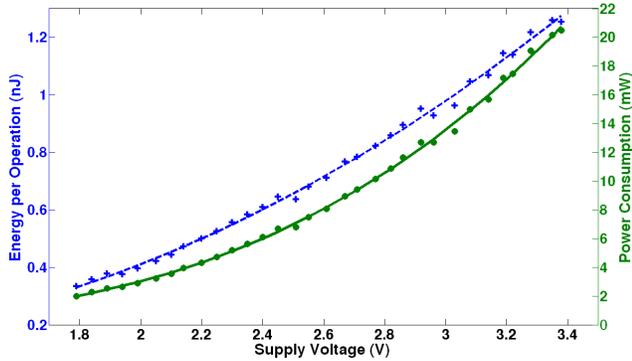


Figure 8: MSP430 power consumption (thick trace, right axis) and energy per operation (dashed trace, left axis) with “ V_{DD} - F_{DCO} pair” scaling.

The data in Figure 8 can be combined with other possible operation scenarios using processor frequencies below the maximum to yield a 3D surface and a fit equation that can predict the power consumption of the MSP430 given any voltage and frequency operation. The surface and fit equation are shown in Figure 9 and Equation 5.

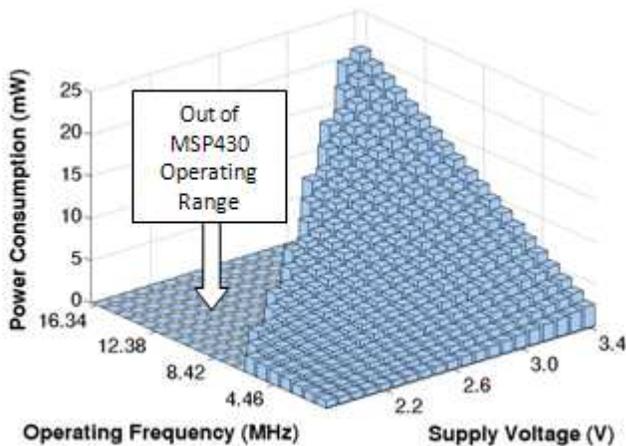


Figure 9: MSP430 power consumption with any given V_{DD} and F_{DCO} .

$$P_{p,mW} = 6.82462 - 5.42187 \cdot V_{DD} - 9.09963 \times 10^{-7} \cdot F_{DCO} + 1.10801 \cdot V_{DD}^2 + 6.52311 \times 10^{-16} \cdot F_{DCO}^2 + 6.17356 \times 10^{-7} \cdot V_{DD} \cdot F_{DCO} \quad (5)$$

This equation can be used to predict the power consumption at any pair, but in most situations, the voltage-frequency pairs from Figure 8 will be used.

In addition to the measurements displayed in Figure 8, the processor was disconnected from the power supply and power consumption was measured once again to get an estimate of 0.55

mW for the external circuitry overhead. This offset will be ignored for many of the following experiments since it is not the focus of this study, but it should be kept in mind that designing more efficient external circuitry could further reduce overall power consumption.

An equation for power consumption of the MSP430 can be extended from that of a general CMOS switching circuit (Equation 2) to involve a constant from external circuitry overheads (D) in the following equation:

$$P_p = C \cdot V_{DD}^2 \cdot F_{DCO} + D \quad (6)$$

Equation 3 can be substituted for F_{DCO} to yield the following:

$$P_p = A \cdot V_{DD}^3 - B \cdot V_{DD}^2 + D \quad (7)$$

When a fit of this form is performed to the power consumption data shown in Figure 8, the following equation gives the power consumption at any voltage (assuming the maximum operating frequency at that voltage):

$$P_{fit} = 0.8575 \cdot V_{DD}^3 - 1.15 \cdot V_{DD}^2 + 0.7646 \quad (8)$$

This fit-line has a Pearson correlation coefficient of 0.999 and is shown as the thick trace in Figure 8. Though the ratio of the V3 and V2 coefficients is not what is expected using Equations 2 and 6, it can be assumed that it fits the actual current consumption of the MSP430.

From the data shown in Figure 8, energy per operation can be calculated by dividing the power consumption values by the F_{DCO} at that point resulting in the “+” data points and dashed fit-line. Again, energy per operation is useful for calculating the break-even cycles.

4.3 Transient Analysis

Tests were conducted to study the transient behavior of the circuit under dynamic voltage shifting conditions. Figure 10 illustrates the overall timing of a voltage shift from 1.8 volts to 3.3 volts and back to 1.8 volts. The top trace is a general purpose I/O pin set up in firmware to instrument the transition process; the lower trace is the actual power supply voltage. At the beginning of the I²C transmission to the digital potentiometer, the instrumentation signal goes high – in this case to the previously established 1.8 volt level. At the conclusion of the I²C sequence, V_{DD} rises to 3.3 volts. V_{DD} is maintained at this level for 2.5ms, then a command is sent to lower the voltage back to 1.8 volts. V_{DD} can be seen to decay back to 1.8 volts over a period of 5 ms following the end of the I²C sequence. This rather protracted decay in voltage is largely due the charge stored on the 4.7 μ F output capacitor, required for stability of the regulator. (Note: this is in the manufacturer’s specification for this part.)

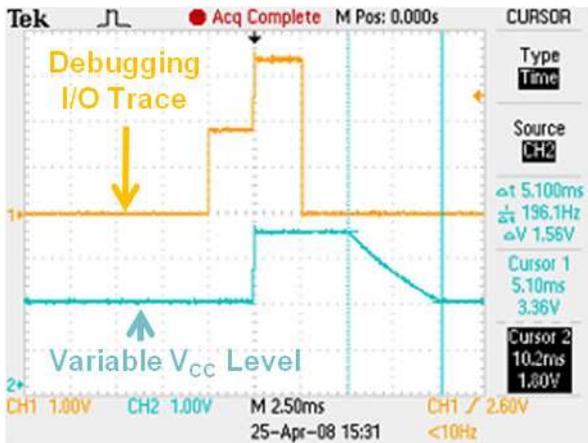


Figure 10: Timing of V_{CC} shifting up then down (bottom = V_{CC} level, top = I/O line for debugging).

The leading edge of the upward voltage transition is shown in Figure 11. Since this transition is being actively driven by the regulator, its rise time is much faster, approximately 25 μ s.

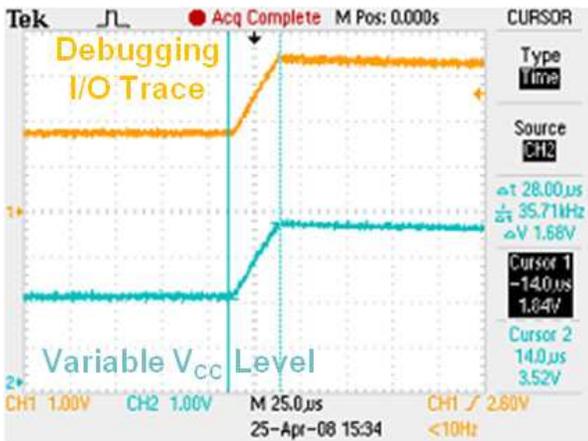


Figure 11: V_{CC} quickly transitioning from 1.8 to 3.3 volts (bottom = V_{CC} level, top = I/O line for debugging).

The data from the scope readings for each voltage transition in steps of 0.3V was then analyzed to determine the settling time for the supply voltage for any transition. Table 1 clearly shows a large time difference between increasing and decreasing V_{DD} that is consistent with the expected charging and discharging rates of the 4.7 μ F capacitor.

Table 1: Settling times for V_{DD} transitions.

Current Voltage	Next Voltage			
	1.8	2.1	2.4	2.7
1.8		4.5 μ s	9.7 μ s	13.7 μ s
2.1	1150 μ s		4.1 μ s	9.8 μ s
2.4	2270 μ s	790 μ s		4.8 μ s
2.7	3230 μ s	1860 μ s	860 μ s	
3	4040 μ s	2660 μ s	1590 μ s	660 μ s
3.3	4940 μ s	3520 μ s	2430 μ s	1430 μ s

A firmware program was designed to switch between two voltages at a time so that oscilloscope readings could be recorded and the transient waveforms could be seen for both increasing and

decreasing V_{DD} . Figure 12 shows the nature of transitions from lower-voltage to higher-voltage operation and back, just as in the transient testing routine.

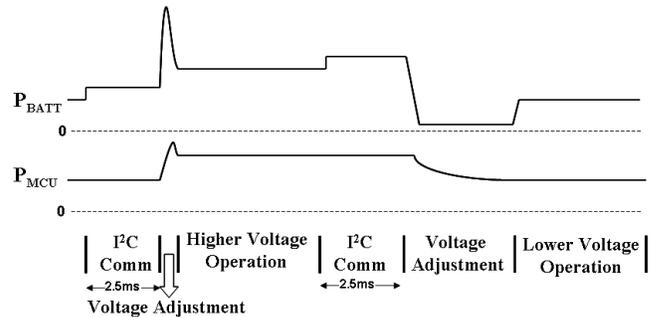


Figure 12: Transient behavior of power consumption during downward and upward voltage shift.

During an I^2C command, the power consumption rises slightly due to the bus activity and the current draw of the passive pull-ups. At the conclusion of the command, the power consumption drops close to 0 while the capacitor on the output of the regulator discharges (approximately 5 ms in this case). As soon as the capacitor voltage decays to the lower level, power consumption resumes at a lesser rate. During an upward transition, there is a slight increase in power consumption in the I^2C communication, as before. This is followed by a sharp (but brief) spike in consumption due to the recharge of the capacitor on the output of the regulator. There is also a slight overshoot of the regulated voltage output, leading to a brief period ($< 10 \mu$ s) of higher power consumption. This is then followed by stable consumption at the higher power level.

From these assumptions about the transient behavior of the system, the following equation can be constructed to model the energy overheads for transitioning down to a lower voltage and back up to the original ($V_1 > V_2$ for all following equations):

$$E_{TRANSITION} = T_{I2C} \left[\left(P_{MSP}(V_1) + \frac{V_1^2}{R_{PULL-UP}} \right) + \left(P_{MSP}(V_2) + \frac{V_2^2}{R_{PULL-UP}} \right) \right] + \frac{1}{2} \cdot C_{REG} \cdot (V_1 - V_2)^2 \quad (9)$$

The first term of the equation encompasses the I^2C communication overhead, including the power required to pull down resistors for communication. The second term is derived from Equation 10 involving the energy required to recharge the regulator's output capacitor and the dissipated energy when discharging the capacitor to a new voltage:

$$C_{REG} \cdot V_1 \cdot (V_1 - V_2) - \frac{1}{2} \cdot C_{REG} \cdot (V_1^2 - V_2^2) = \frac{1}{2} \cdot C_{REG} \cdot (V_1 - V_2)^2 \quad (10)$$

Equation 9 represents the ideal case where there is no overhead in the regulator for switching between voltage levels, and these effects will be ignored from this point on since the efficiency of the external circuitry is not the primary focus of this study.

The switching overhead can be used to create an ideal equation for break-even switching cycles:

$$N \cdot E_{perOP}(V_1) = N \cdot E_{perOP}(V_2) + E_{TRANSITION} \quad (11)$$

Equation 11 can be solved for N at any given voltage pair. N is the minimum number of cycles that would not result in energy loss switching to V_2 and back to V_1 (break-even cycles). Table 2 shows the break-even cycles in kilo-cycles using the data shown in Figure 8 and the current system setup ($T_{I2C} = 2.5\text{ms}$, $R_{PULL-UP} = 10\text{k}\Omega$).

Table 2: Break-even processor cycles x 10^3 with current system settings.

		V2 (V)							
		1.8	2	2.2	2.4	2.6	2.8	3	3.2
V1 (V)	1.9	293.32							
	2	229.96							
	2.1	146.34	382.62						
	2.2	109.77	195.06						
	2.3	92.81	140.88	460.90					
	2.4	84.54	117.97	261.89					
	2.5	84.06	113.17	223.92	1279.00				
	2.6	77.19	97.83	161.72	379.06				
	2.7	73.41	89.37	133.58	242.46	653.68			
	2.8	71.13	84.02	117.26	186.00	348.93			
	2.9	68.74	79.02	103.99	149.32	232.62	670.48		
	3	71.83	82.11	107.03	151.76	232.35	626.81		
	3.1	69.91	78.25	97.63	129.53	179.47	337.19	728.95	
3.2	70.31	77.75	94.75	121.56	161.05	268.83	462.58		
3.3	69.37	75.61	89.51	110.35	138.97	206.35	300.06	831.16	

The break-even cycles increase dramatically when V1 and V2 are very close in magnitude, which suggests that even though the overhead of switching a small amount is low, the power benefits of operating at an only slightly lower voltage are limited. In addition, the overhead of the control signals to switch voltage-frequency pairs is constant regardless of the switching magnitude. The data shown in Table 2 can be used to construct a second order polynomial fit to calculate the expected number of break-even cycles and make informed decisions about whether to switch to a new V_{DD} state. Figure 13 shows the fitted values with a r^2 value greater than .99, indicating an accurate representation of the empirical data.

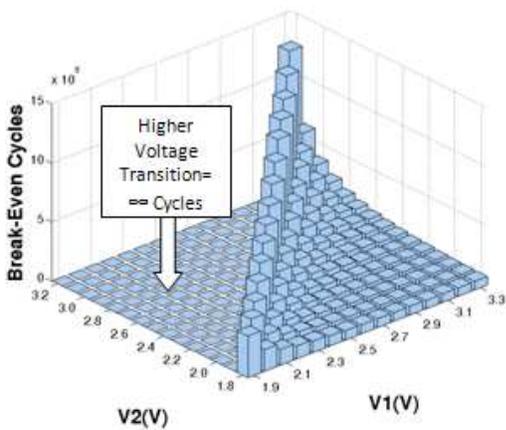


Figure 13: Calculated break-even cycles using polynomial fit of energy per operation values.

Given the frequencies paired with the voltages, Table 3 shows that typical break-even times for DVFS scaling are in the range of 10 ms to 50 ms. Such times are entirely consistent with the requirements of a large segment of BASN applications, including human motion assessment. Even in activities such as walking, the range of observed frequencies is typically much less than 10 Hz, and the corresponding periods are greater than 100 ms.

Table 3: Break-even times (ms) with current system settings.

		V2 (V)							
		1.8	2	2.2	2.4	2.6	2.8	3	3.2
V1 (V)	1.9	48.838							
	2	38.288							
	2.1	24.366	52.128						
	2.2	18.276	26.575						
	2.3	15.453	19.193	53.14					
	2.4	14.076	16.072	30.19					
	2.5	13.996	15.419	25.82	127.8				
	2.6	12.853	13.329	18.64	37.876				
	2.7	12.223	12.176	15.4	24.226	57.633			
	2.8	11.842	11.447	13.52	18.585	30.764			
	2.9	11.445	10.766	11.99	14.92	20.51	52.894		
	3	11.96	11.187	12.34	15.164	20.486	49.448		
	3.1	11.64	10.66	11.26	12.942	15.824	26.601	52.031	
3.2	11.707	10.593	10.92	12.146	14.199	21.208	33.018		
3.3	11.551	10.301	10.32	11.027	12.252	16.279	21.417	54.17	

The switching overhead factors that drive the break-even cycles are C_{REG} and T_{I2C} , as defined in Equation 9. In the current system, $C_{REG} = 4.7\mu\text{F}$, but this is dependent on the specifications of the voltage regulator used. Figure 14 uses four different voltage transitions to demonstrate the effect of C_{REG} on break-even cycles.

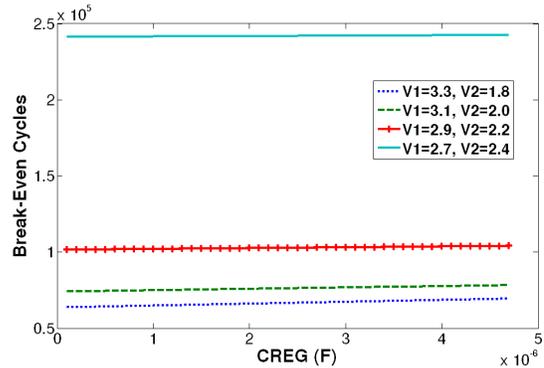


Figure 14: Effect of C_{REG} on break-even cycles.

In the current system, $T_{I2C} \approx 2.5\text{ms}$, but this is determined by the limits of the digital potentiometer, and other methods could be used to reduce this time. Figure 15 uses four different voltage transitions to demonstrate the effect of T_{I2C} on break-even cycles.

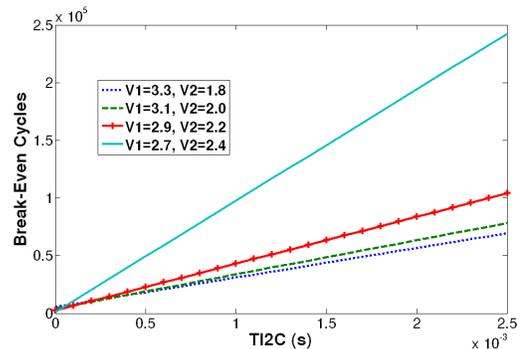


Figure 15: Effect of T_{I2C} on break-even cycles.

With further optimization of supply voltage transition times, break-even times could be improved by a factor of 10 or more. A comparison of Figure 15 to Figure 14 suggests that communication to and from an adjustable regulator (T_{I2C}) should be the main focus of further research since it plays a larger part than C_{REG} in reducing break-even times.

5. IMPACT AND CONCLUSION

Given that the break-even times are significantly shorter than the dynamics of most BASN applications, DVFS for COTS processors represents a viable approach to reduce energy consumption, especially in the domain of applications where there are long periods of low activity that can benefit from lower data processing overhead. Consider a typical medical application such as tremor monitoring. Relevant factors may include a patient's medication schedule, time of day, and normal activities such as walking or eating. There may be periods of 10's of milliseconds to many seconds in which activity levels are so low that virtually no signal processing is required other than basic filtering and thresholding; such operations may be processed at a relatively low clock rate and a correspondingly low supply voltage. When a tremor is detected, the processor can increase its rate as necessary. While our simple hardware requires 2.5 ms to complete a voltage shift, this may be drastically reduced with suitable hardware, and we have shown that this is the dominant factor in determining the number of break-even cycles for a DVFS environment. In addition, it is possible to precalculate the relationships for the break-even surfaces and store them in lookup tables for fast decision making in a typical on-node processing environment.

This research is timely given that several manufacturers (e.g. Linear Technology, Texas Instruments, and Analog Devices) are releasing low power multiple output voltage regulators that will facilitate DVFS on the types of processor platforms under discussion. A clear hole in this tool chain is the lack of a simple and efficient mechanism to switch between voltage levels, but this could be a productive area for future research.

DVFS is only one piece in a larger puzzle in dynamic system adjustment for BASNs, including resolution scaling, compression and DSP techniques, etc. [13, 14]. COTS-DVFS techniques can provide significant power savings without having to design and fabricate custom chips, thereby facilitating inexpensive, low volume systems without a significant loss in power efficiency regardless of the highly dynamic conditions present in BASNs. By allowing for "just-in-time" computing on COTS components, a better tradeoff can be made between system power consumption and application/sensing fidelity. In addition, current/power sensing capabilities promote self-aware control schemes showing promise for autonomous intelligent sensor nodes. Finally, the regulator and power sensing circuitry could be put on an ASIC with or without a processor core allowing for even greater savings in power, size, and integration in future BASN architectures. Overall, COTS-DVFS systems provide a flexible research platform for exploration of power-fidelity tradeoffs in new application spaces for BASNs.

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