On Two-Layer Hierarchical Networks How Does the Brain Do This?

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Abstract. In this paper our aim is to identify layered hierarchical generic network topologies which could closely mimic brain's connectivity. Recent analyses have compared the brain's connectivity (based both on a cortical-equivalent Rent's rule and on neurological data) with well-known network topologies used in supercomputers and massively parallel computers (using two different interpretations of Rent's rule). These have revealed that none of the well-known computer network topologies by themselves are strong contenders for mimicking the brain's connectivity. That is why in this paper we perform a high-level analysis of two-layer hierarchical generic networks. The range of granularities (*i.e.*, number of gates/cores/neurons) as well as the *fan-ins* and the particular combinations of the two generic networks which would make such a mimicking achievable are identified and discussed.

Keywords: Connectivity, interconnect topology, network topology, network-on-chip, communication, nanotechnology, nano-architecture, Rent's rule, neural networks, brain.

1 Introduction

Interconnection is probably the most challenging problem facing the development of tera-scale, *i.e.*, having 10^{12} devices, (multi-/many-core) systems [1]. The problem is that crossbar and other specialized network topologies do not scale well to 1000s of cores. As the number of cores increases the number of interconnections and their (total) length should increase only (very) slowly. At the same time, interconnects' absolute dimensions decrease and create problems imposed by their physical size [2]. With on the order of 10^{10} neurons and 10^{14} synaptic connections, the brain certainly exhibits a highly optimized interconnection scheme. Structures in the brain are characterized by massive interconnections, but contrary to common thought most of these are highly local with a sparse global interconnection scheme [3].

In this paper we will use a top-down approach for analyzing two-layer hierarchical generic networks which could closely mimic brain's connectivity by: (*i*) trying to

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identify an optimal two-layer hierarchical solution; (*ii*) extending our search by taking into account generic (Rent's rule based) types of networks; and (*iii*) considering both multiple- as well as single-wire connections for the (second) global network. Conclusions and future directions for research are ending the paper.

2 Classical Network Topologies

Many topological characteristics of networks have been explored over the years. Their development was effectively stimulated by the evolution of supercomputers. Characteristics such as *degree*, *diameter*, *number of links*, and many other cost functions have been computed and reported for network topologies such as: crossbar, binary hypercube, torus, generalized hypercube, spanning bus hypercube, hierarchical cubic network, cube connected cycle, hyper-deBruijn, folded Peterson, hyper-mesh, to name but a few. These have long been advocated (and some even used) for massively parallel computing and supercomputers. A revived interest is apparent due to the current evolution towards parallelism, which is driven by the advancement of many-/multi-cores processors. The relationships between the number of processing elements (also known as network *size*, or equivalently N_{PROC}, or simply N) and N_{CONN} (number of links) for various network topologies are widely referenced in the literature [4] (see Table 1). As can be seen from Table 1, almost all of them have connectivity complexity of the order $O(N\log N)$ with two exceptions. The cube connected cycles (CCC) has a connectivity which grows only linearly $O(N)$ with the number of nodes N (more precisely $N_{CONN} = 3N/2$). Additionally, the crossbar (XB)—which is one of the highly advocated in the growing nanoarchitecture community due to expected ease of fabrication—has $N_{CONN} = (N^2–N)/2$, being $O(N^2)$.

Table 1. Topological characteristics of classical computer networks

Network	Size N (N_{PROC})	Connections N_{CONN}
Cube Connected Cycles	$c\,2^n$	$3N/2$
Spanning Bus Hypercube	w^D	$N\log_w N\,/w$
Torus	w^n	$N\log_w N$
Hyper-Mesh	w^n	$N\log_w N$
Generalized Hypercube	w^n	$N\log_w N \times(w–1)/2$
Hierarchical Cubic Network	2^{2n}	$N\log_2 N\,/4 + N/2$
Hyper-deBruijn	2^{n+c}	$N\log_2(N - c + 4)/2$
Binary Hypercube	2^n	$N\log_2 N\,/2$
Mesh Hypercube	$l^2\,2^n$	$N(\log_2 N + 3)/2$
Folded Peterson	10^n	$3N\log_{10} N\,/2$
Crossbar	N	$N(N - 1)/2$

Fig. 1 shows a log-log plot of all these networks, including Rent's rule average (as a black dotted line) and Rent's rule range of values (as a yellow area) [12]. This plot shows that: (*i*) almost all the classical network topologies follow quite closely Rent's rule average; (*ii*) CCC seems to be the strongest contender; while (*iii*) apparently XB is the weakest solution (as exhibiting the steepest slope).

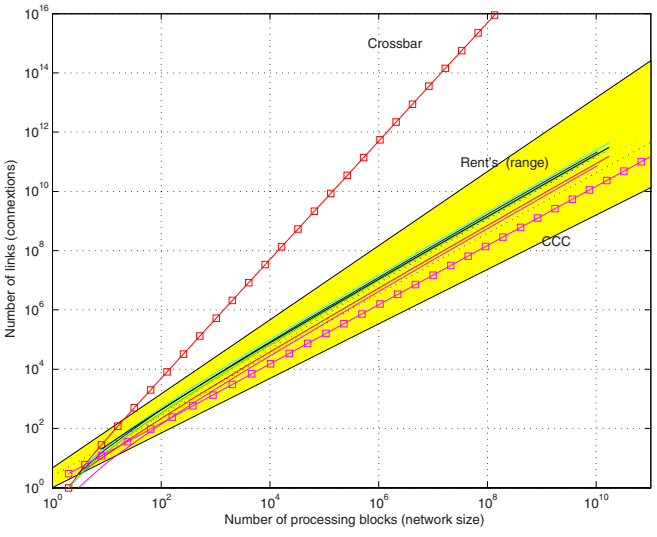

Fig. 1. N_{CONN} versus *size* for Rent's rule (black dotted line) and its range of values (yellow) together with many of the well-known network topologies (crossbar and cube connected cycles are the two extremes)

3 Brain's Connectivity

By looking at nature, one finds that the mammalian brain is one of (if not) the most efficient network of processing elements (currently) known to mankind: on the order of 10^{10} processing elements (*i.e.*, neurons) and almost 10^{14} connections (*i.e.*, synapses), let alone that each synapse has an associated (low-precision analog) weight [5]. There is no doubt that mammals' brains have evolved to operate efficiently—the unknown(s) being the optimization cost(s). A smaller brain will certainly require fewer materials and less energy for 'construction,' 'maintenance,' and 'operation' (*i.e.*, lighter skeletal elements and muscles, and reduced energy). Obviously, the size of a nervous system could be reduced by:

- reducing the number of neurons (a certain minimum is still required for adequate functioning) [6];
- reducing the average size of neurons (*e.g.*, by reducing their *fan-in* and/or *fan-out*);
- laying out the neurons such as to reduce (optimize) the (total wiring) lengths of their (inter)connections [3], [6], [7].

At the highest level, the brain is segregated into white (of volume W) and gray (of volume G) matter. White matter contains long axons implementing long-range connections (*i.e.*, global communications) between cortical areas. In human brain, these long axons occupy about 44% of the white matter volume, hence $N_{CONN} \sim 0.44W$. On the other hand, the gray matter contains cell bodies, dendrites, and axons for information processing and local communication [8]. Axons and dendrites

constitute about 60% of the gray matter, which suggest that $N_{CONN} \sim 0.6G$, and also that $N_{NEU} \sim 0.4G$. This indicates a quite high degree of local communication (*i.e.*, analogous to the implementation of local area networks). This 60% wiring fraction is (probably) optimizing the (local) delays by balancing transmission speeds (and also energy) as well as component densities. In the case of neurons, reducing the diameter of axons reduces the speed at which signals travel, hence, increasing their delays. But, this also reduces axon volume, allowing for packing neurons closer together, hence tending to shorten delays. Although such a view of the brain is certainly simplistic, it still captures the fact that *the brain could be modeled as a hierarchical communication network consisting of (at least) two sub-networks: a global and a local one*.

For various mammalian species, as brain size increases, the volume W of the white matter beneath the cortex tends to increase faster than the volume G of the cortical gray matter according to a power law [9]:

$$\log_{10} W = (1.23 \pm 0.01) \log_{10} G - (1.47 \pm 0.04) \tag{1}$$

$$W = 10^{-1.47} \times G^{1.23} \tag{2}$$

As a first approximation this implies that $N_{CONN} = k_B \times N^{p_B}$, being a cortical (equivalent of) Rent's rule [10], [11], with $k_B = 10^{-1.47}$ and $p_B = 1.23$ (as it relates N_{CONN}, *i.e.* axons in W, to N_{NEU}, the number of neurons in G).

Just like the wires connecting components in semiconductor chips, the connections between neurons occupy a substantial fraction of the total volume, and the 'wires' (axons and dendrites) are expensive to operate as dissipating energy during signaling. In fact, although the human brain represents only 2% of the total body weight, it consumes 20% of its resting energy—which is obviously quite expensive! However, nature has an important advantage over electronic circuits. In mammals' brains components are connected in 3D space, whereas even the most advanced microprocessor chips use only a small number of layers of planar wiring. This could be (one of) the reason(s) why wiring occupies 60% of the whole brain's volume—which is still considerably less than the 90% of today's VLSI chips.

Still, the approach presented above is not too accurate as N_{CONN} would need to include not only the global connections $0.44W$, but also the local ones (in the gray matter), which are about $0.6G$. On top of these, the new interpretation of Rent's rule counts each connection twice (once as input and also as output), hence $N_{CONN} \sim 2(0.44W + 0.6G)$. This interpretation leads to the more accurate:

$$N_{CONN} = 0.092 N_{NEU}^{1.23} + 3N_{NEU} \,. \tag{3}$$

This hardly changes anything if at all, as the growth of N_{CONN} is still given by $p_B \approx 1.23$ (eqs. (2) and (3)).

Additionally, from the work of Lanzerotti, Fiorenza, and Rand [12] (based on POWER4 units), one could estimate the average Rent values as $k_R = 2.835$ and $p_R = 1.023$.

Finally, in Fig. 2 we have plotted:

- the data for several IBM POWER4 units [12] (as mentioned above); as well as
- the brain using neurological data for human (N_{NEU} = 2...3×10^{10}, N_{CONN} = 1.5...2.5×10^{14}), macaque (N_{NEU} = 2×10^{9}, N_{CONN} = 2.2×10^{13}), cat (N_{NEU} = 1.08×10^{9}, N_{CONN} = 9.05×10^{12}), rat (N_{NEU} = 6.5×10^{7}, N_{CONN} = 5.45×10^{11}), and mouse (N_{NEU} = 1.6...2.6×10^{7}, N_{CONN} = 1...2.2× 10^{11}).

These results show that the brain has a much higher connectivity than suggested by eqs. (2) or (3). This also was partly to be expected, as eq. (2) considers only the connections in the white matter (*i.e.*, it ignores local connections in the gray matter). Fig. 2 also shows that the brain's average based on neurological data (red dotted line in Fig. 2) is parallel to Rent's average (black dotted line), which is due to the new interpretation of Rent's rule [12]. Basically, Rent's average (black dotted line) would correspond to *fan-in* = 4, while neurological data (red dotted line) correspond to a *fan-in* = 8000.

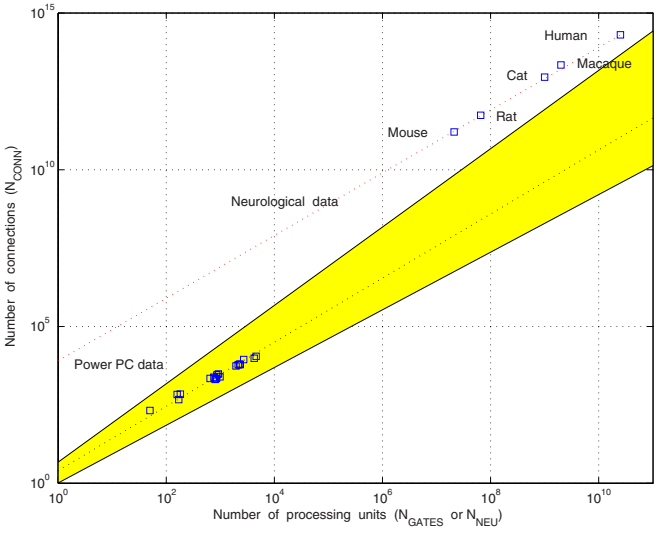

Fig. 2. N_{CONN} versus *size* for Rent's rule (black dotted line) and its range of values (yellow) together with data from the POWER PC (blue squares on Rent's average), as well as neurological data

4 Two-Layer Hierarchical Networks

Previous results [13] have shown that the well-known computer network topologies fall short of being strong contenders for mimicking the brain's connectivity.

Hierarchical solutions when applied to emerging many-to-1000's core scenario can be understood as follows. Inside each core the connections form *a local network*, while among the cores connections form *a global network*. For any two-layer hierarchical network the total number of connections can be calculated exactly as:

$$N_{CONN} = N_{PROC} \times N_{CONN}(\text{per core}) + N_{CONN}(\text{among cores}) \times [1 \ldots N_{GATES}(\text{per core})]. \quad (4)$$

Here N_{CONN} is the total number of connections, N_{PROC} is the number of processors (cores) inside a single chip, and N_{CONN}(per core) is the number of connections inside a core. This equation has two parts: the first part is the sum of all connections representing the local networks; while the second part is the sum of all connections forming the global (among the cores) network. The multiplication factor [1…N_{GATES}(per core)] represents the number of wires which are used in each of the connections forming the global (inter-core) network. Hence, if this factor is 1 the global network will use only single-wire (serial) connections, while otherwise the global network will be made of multiple-wire (parallel) connections.

Let us suppose that N is the total number of gates the chip has, and that m (= N_{GATES}) is the number of gates inside each core. This implies that the number of cores is $N_{PROC} = N/m$ (this number has to be an integer). Additionally, we shall consider that a generic network has a connectivity of the form $X^{1+\alpha}$ (power law derived from the classical interpretation of Rent's rule), where X is the number of gates and α is between 0 and 1 (with 0 corresponding to a CCC-type of network, and 1 corresponding to a XB-type of network). Similarly, the second (global) network will have a connectivity of the form $Y^{1+\beta}$ ($0 \le \beta \le 1$). For example, if $\alpha = \beta = 1$ this would mean that the two-layer hierarchical network could be an XB-of-XBs, while if $\alpha = \beta = 0$ the two-layer hierarchical network could be a CCC-of-CCCs. A combination like *e.g.* $\alpha = 1$ and $\beta = 0$ could be represented by a CCC-of-XBs. What would fractional values of α and β represent? Obviously, two networks satisfying $X^{1+\alpha}$ and $Y^{1+\beta}$. And which networks would these be? Here the answer is more nuanced, but one possible solution would be that these are random dynamical networks [14] satisfying the above mentioned growth rates.

Using two such generic networks, a local one as $m^{1+\alpha}$ and a global one as $(N/m)^{1+\beta}$ in eq. (4), and considering the extreme case when the multiplication factor is $m = N_{GATES}$(per core), we obtain:

$$N_{CONN} \le (N/m)\times m^{1+\alpha} + (N/m)^{1+\beta}\times m = N\times m^{\alpha} + N\times(N/m)^{\beta}. \quad (5)$$

Solving for β gives:

$$N_{CONN}/N = m^{\alpha} + (N/m)^{\beta} = F_{IN\_avg}$$

$$\beta = \log(F_{IN\_avg} - m^{\alpha}) / (\log N - \log m). \quad (6)$$

Eq. (6) is plotted in Fig. 3 for different values of *fan-ins* (4, 40, 400 and 4000) while varying α in steps of 0.1 and m in between 1 and 10,000, when $N = 10^{10}$. Our interest here is to identify the minimum values of β for all possible (α, m) combinations—while *in general one might want to minimize the total wire length.* The most obvious combination is $\alpha = 1$ and $m = fan\text{-}in$, which makes $\beta = 0$, but any $m^{\alpha} = fan\text{-}in$ will do. *Fan-in* = 4 is the current standard in VLSI, with 40, 400 and 4000 being simulated for analysis purpose only as: (*i*) multi-/many-cores (for future 1000s of cores), would have to have higher *fan-ins* (say 32, 64, etc.); (*ii*) neurons are estimated to process about 8000 inputs (on average), being of interest when trying to emulate the brain. Fig. 3 shows that for $m^{\alpha} = fan\text{-}in$ significant improvements are possible as β drops to zero!

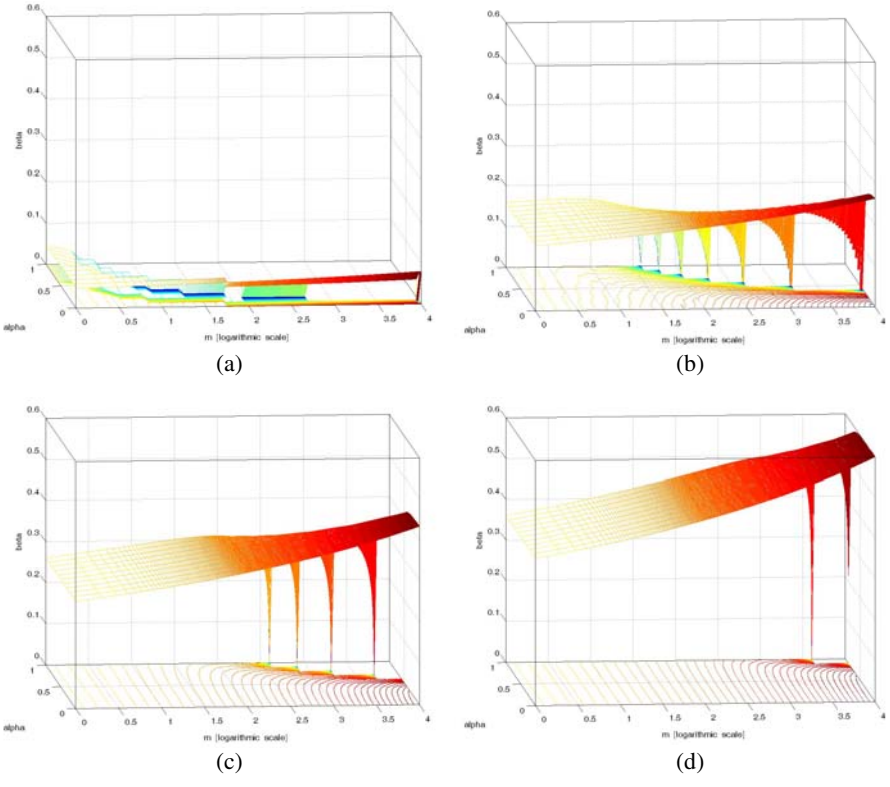

Fig. 3. β as a function of m and α when m-wide busses are used for the global connections (10^{10} connections), and for average *fan-ins* of: (a) 4 (current VLSI circuits); (b) 40; (c) 400; (d) 4000 (half of the neurons' average *fan-in*)

When considering a single-wire (multiplication factor of 1) instead of an m-bit bus $N_{\mathrm{CONN}} = (N/m) \times m^{1+\alpha} + (N/m)^{1+\beta}$ and the solution becomes:

$$\beta = [\log(F_{IN\_avg} - m^{\alpha}) + \log m] \,/\, (\log N - \log m). \tag{7}$$

This is shown in Fig. 4 for the same conditions (namely *fan-in* = 4, 40, 400, and 4000, while varying α in steps of 0.1 and m in between 1 and 10,000, when $N = 10^{10}$). These show a slightly different picture, with β growing with increasing m. Still, the same α and m combinations ($m^{\alpha} = fan\text{-}in$) minimize β to $\log(fan\text{-}in^{1/\alpha})/\log(N/fan\text{-}in^{1/\alpha})$.

The results presented here support an organization of the brain in hypercolums. If a neuron has a *fan-in* of 8000, it follows that for $\alpha = 1$ (*i.e.*, locally a fully connected network) and $m = 8000$ we have $\beta = 0$. Hence, 80 minicolumns of about 100 neurons each would be a possible solution as $m = 80 \times 100 = 8000$ (a hypercolumn). These numbers are consistent with published data [15]–[17]. Even if each neuron would use 7999 synapses for the local connections, and only 1 synapse for the global connections, the aggregate bandwidth of a hypercolumn would be that of a whooping 8000-wide bus!

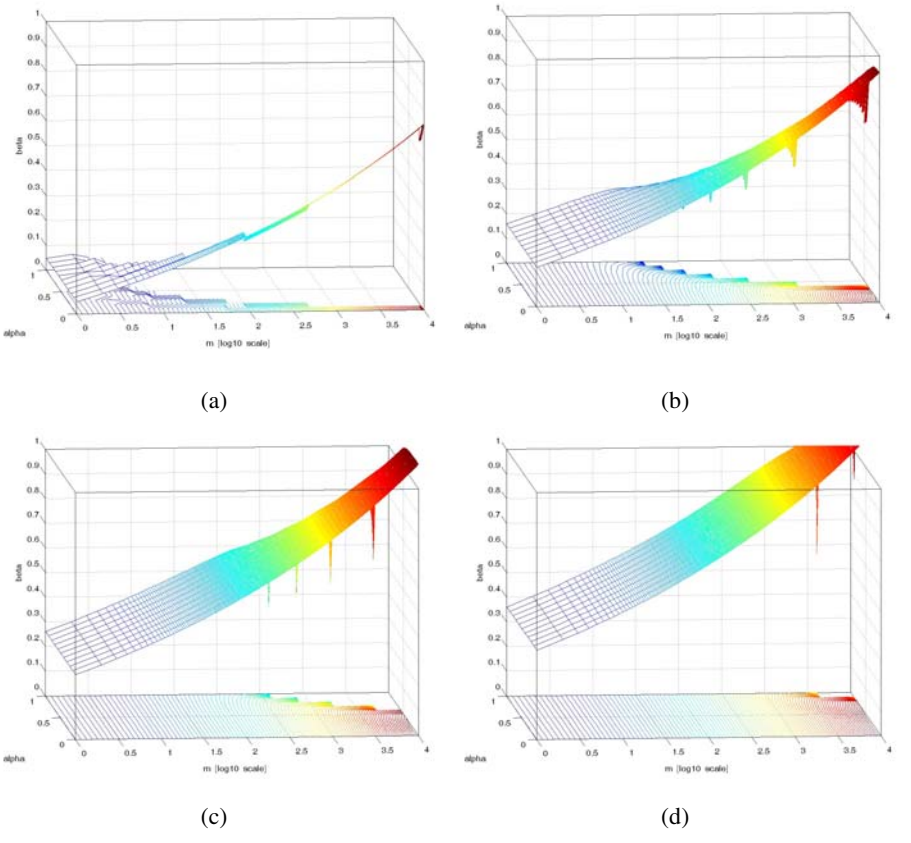

Fig. 4. β as a function of m and α when single wires are used for the global connections (10^{10} connections), and for average *fan-ins* of: (a) 4 (current VLSI circuits); (b) 40; (c) 400; (d) 4000 (half of the neurons' average *fan-in*)

4 Conclusions

The results presented in this paper show that two-layer hierarchical generic networks are able to mimic brain's connectivity, while particular (*fan-in*, m, α) combinations can significantly reduce the complexity of the global network (β). One possible solution for m close to *fan-in* is to rely on a highly connected ($\alpha = 1$) local network (*e.g.*, a $fan\text{-}in^{1/2} \times fan\text{-}in^{1/2}$ crossbar), followed by a sparsely connected (β between 0 and $\log(fan\text{-}in^{1/\alpha})/\log(N/fan\text{-}in^{1/\alpha})$) global network. As an example, a 1024-core chip with a *fan-in* of 64 per core, should use 8×8 crossbars as local (first layer) networks, followed by a sparse 64-bit wide global (second layer) network.

Future work should concentrate on closely estimating the length of the wires (connections) and optimizing results like the ones presented here with respect to the (total) wire length. Results like [18]–[23], should be revisited, and should be followed by

thorough re-evaluations of the tradeoffs between *performance-area-power-energy* [24]–[26] versus reliability [27]–[33], as well as by investigating these in the context of alternate communication techniques, like those discusses in [34]–[37], or by photonic ones [38].

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